Please type a plus sign (+) inside this box [+]

PTO/SB/05 (12/97)
Approved for use through 09/30/00. OMB 0651-0032
Patent and Trademark Office: U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

UTILITY PATENT APPLICATION TRANSMITTAL

(Only for new nonprovisional applications under 37 CFR 1.53(b))

Attorney Docket No. 03401.P090 Total Pages 3

First Named Inventor or Application Identifier Douglas S. Ondricek

Express Mail Label No. EL 164 803 864 US

ADDRESS TO: **Assistant Commissioner for Patents**
Box Patent Application
Washington, D. C. 20231

APPLICATION ELEMENTS
See MPEP chapter 600 concerning utility patent application contents.

1. X Fee Transmittal Form
(Submit an original, and a duplicate for fee processing)

2. X Specification (Total Pages 37)
(preferred arrangement set forth below)
- Descriptive Title of the Invention
- Cross References to Related Applications
- Statement Regarding Fed sponsored R & D
- Reference to Microfiche Appendix
- Background of the Invention
- Brief Summary of the Invention
- Brief Description of the Drawings (if filed)
- Detailed Description
- Claims
- Abstract of the Disclosure

3. X Drawings(s) (35 USC 113) (Total Sheets 17)

4. X Oath or Declaration (Total Pages 4)

a. ___ Newly Executed (Original or Copy)

b. ___ Copy from a Prior Application (37 CFR 1.63(d))
(for Continuation/Divisional with Box 17 completed) **(Note Box 5 below)**

i. ___ DELETIONS OF INVENTOR(S) Signed statement attached deleting inventor(s) named in the prior application, see 37 CFR 1.63(d)(2) and 1.33(b).

5. ____ Incorporation By Reference (useable if Box 4b is checked)
The entire disclosure of the prior application, from which a copy of the oath or declaration is supplied under Box 4b, is considered as being part of the disclosure of the accompanying application and is hereby incorporated by reference therein.

6. ____ Microfiche Computer Program (Appendix)

7. ____ Nucleotide and/or Amino Acid Sequence Submission
(if applicable, all necessary)
a. ____ Computer Readable Copy
b. ____ Paper Copy (identical to computer copy)
c. ____ Statement verifying identity of above copies

ACCOMPANYING APPLICATION PARTS

8. _____ Assignment Papers (cover sheet & documents(s))
9. _____ a. 37 CFR 3.73(b) Statement (where there is an assignee)
_____ b. Power of Attorney
10. _____ English Translation Document (if applicable)
11. _____ a. Information Disclosure Statement (IDS)/PTO-1449
_____ b. Copies of IDS Citations
12. _____ Preliminary Amendment
13. X Return Receipt Postcard (MPEP 503) (Should be specifically itemized)
14. _____ a. Small Entity Statement(s)
b. Statement filed in prior application, Status still proper and desired
15. _____ Certified Copy of Priority Document(s) (if foreign priority is claimed)
16. _____ Other: Copy of postcard with Express Mail Certificate of Mailing

17. **If a CONTINUING APPLICATION,** check appropriate box and supply the requisite information:
___ Continuation ___ Divisional X Continuation-in-part (CIP)
of prior application No: 09/205,502 filed 12-4-98

18. **Correspondence Address**
_____ Customer Number or Bar Code Label _____
(Insert Customer No. or Attach Bar Code Label here)
or
X Correspondence Address Below

NAME James C. Scheller, Jr.
BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP
ADDRESS 12400 Wilshire Boulevard
Seventh Floor
CITY Los Angeles STATE California ZIP CODE 90025-1026
Country U.S.A. TELEPHONE (408) 720-8598 FAX (408) 720-9397

PTO/SB/05 (12/97)
Approved for use through 09/30/00. OMB 0651-0032
Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

03401.P090

UNITED STATES PATENT APPLICATION

FOR

METHOD FOR PROCESSING AN INTEGRATED CIRCUIT

INVENTORS:

DOUGLAS S. ONDRICEK
DAVID V. PEDERSEN

PREPARED BY:

BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN
12400 WILSHIRE BOULEVARD
SEVENTH FLOOR
LOS ANGELES, CA 90025-1026

(408) 720-8598

EXPRESS MAIL CERTIFICATE OF MAILING

"Express Mail" mailing label number: EL 164 803 864 US

Date of Deposit: March 1, 1999

I hereby certify that I am causing this paper or fee to be deposited with the United States Postal Service "Express Mail Post Office to Addressee" service on the date indicated above and that this paper or fee has been addressed to the Assistant Commissioner for Patents, Washington, D. C. 20231

Connie Thayer
(Typed or printed name of person mailing paper or fee)

Connie Thayer
(Signature of person mailing paper or fee)

3-1-99
(Date signed)

METHOD FOR PROCESSING AN INTEGRATED CIRCUIT

BACKGROUND OF THE INVENTION

Related Applications

This application is a continuation-in-part of co-pending, commonly assigned United States Patent Application Serial No. 09/205,502, filed December 4, 1998, entitled "Socket for Mating with Electronic Component, Particularly Semiconductor Device with Spring Packaging for Fixturing, Testing, Burning-In." That application is incorporated herein in full by reference.

This application is related to the patent application titled "Method for Mounting an Electronic Component" and to the patent application titled "Method for Processing an Integrated Circuit" which are being filed concurrently herewith.

Field of the Invention

The present invention relates in general to electronic assemblies and the testing thereof. More specifically, the present invention relates to a method and apparatus for the transport and handling of die from an original wafer to a test board, a printed circuit board, and/or a final product substrate.

Description of Related Art

The subject of chip scale packaging has been the focus of intense study in the industry for many years. One very promising technology involves securing small, resilient members onto a suitable substrate and using these members to effect contact between an active device and other circuitry. Methods are known for making such resilient interconnection elements used for microelectronics, and for fabricating spring contact elements directly on semiconductor devices. A particularly useful resilient interconnection element comprises a free standing spring contact element secured at one end to an electronic device and having a free end standing away from the electronic device so as to readily contact a second

electronic device. See, for example, United States Patent 5,476,211, entitled "Method for Manufacturing Electrical Contacts, Using a Sacrificial Member."

A semiconductor device having spring contact elements mounted thereto is termed a springed semiconductor device. A springed semiconductor device may be interconnected to an interconnection substrate in one of two principal ways. It may be permanently connected, such as by soldering the free ends of the spring contact elements to corresponding terminals on an interconnection substrate such as a printed circuit board. Alternatively, it may be reversibly connected to the terminals simply by urging the springed semiconductor device against the interconnection substrate so that a pressure connection is made between the terminals and contact portions of the spring contact elements. Such a reversible pressure connection can be described as self-socketing for the springed semiconductor device. A discussion of making semiconductors with spring packaging (MicroSpring™ contacts) is found in United States Patent 5,829,128, issued November 3, 1998, entitled "Method of Mounting Resilient Contact Structures to Semiconductor Devices." A discussion of using and testing semiconductors with MicroSpring™ contacts is disclosed in U.S. Patent Application Serial No. 09/205,502, filed December 4, 1998, entitled "Socket for Mating with Electronic Component, Particularly Semiconductor Device with Spring Packaging, for Fixturing, Testing, Burning-In or Operating Such a Component", and assigned to the assignee of the present invention.

The ability to remove a springed semiconductor device from a pressure connection with an interconnection substrate would be useful in the context of replacing or upgrading the springed semiconductor device. A very useful object is achieved simply by making reversible connections to a springed semiconductor device. This is also useful for mounting, temporarily or permanently, to an interconnection substrate of a system to burn-in the springed semiconductor device or to ascertain whether the springed semiconductor device is measuring up to its

specifications. As a general proposition, this can be accomplished by making pressure connections with the spring contact elements. Such contact may have relaxed constraints on contact force and the like.

In a typical manufacturing process, a wafer is subjected to limited testing to identify gross functionality or non-functionality of individual components on the wafer. The functional individual semiconductor components or die are then packaged for further burn-in and more comprehensive testing. The packaging process is both expensive and time consuming.

Using the MicroSpring contacts for interconnects provides fully testable die while still on the wafer. One preferred method of testing the die is to singulate them, then move them through a more or less typical test flow as is currently performed on packaged devices. A key difference is that the die are already packaged once singulated from the wafer, but current testing equipment is not adapted for use with such devices.

To achieve this, a chip level part or IC die could be placed into a carrier once it is diced from the original wafer. The carrier could then transport the die to the test board for burn-in tests, for example. Once all die in the carrier pass inspection, the carrier could then be used to transport and mount the die onto the printed circuit board or final product substrate.

Such a carrier would be particularly useful for die which include MicroSpring contacts, or similar contacts. Such a carrier also would be useful for traditional die for making contact with a test apparatus or final product that includes a suitable connection mechanism. A test apparatus or final product including MicroSpring contacts would be particularly useful for connecting to traditional die.

A chip level carrier would provide several advantages over the art. First, an individual die would be tested and could be replaced if it failed testing. Second, a chip level carrier could incorporate a tracking mechanism that could track each

individual die, storing relevant information on the carrier for monitoring and tracking. Third, a chip level carrier allows for easy handling of numerous dies and protects the dies and their spring contacts during transportation, storage and use. Further, a carrier could limit the amount of compression the spring contacts on the die under test underwent, which may be less than the compression allowed during subsequent primary use of the die. The limitation of the compression could be achieved through design decisions to determine a maximum allowable compression for the spring contacts during the testing phase. Then, different limits can be adopted for actual use. This feature would increase the "travel" life of the spring.

SUMMARY OF THE INVENTION

The present invention relates to methods for processing at least one die which comprises an integrated circuit.

In one example of a method of the invention, an identification code is applied to a carrier. A singulated die is deposited into the carrier which holds the singulated die. The singulated die comprises an integrated circuit. The identification code may be applied to the carrier before or after depositing the singulated die into the carrier. The carrier may be used in testing the singulated die and may include a plurality of singulated die or just one singulated die.

In another example of a method of the invention, an identification code is applied to a die. The die is deposited into a carrier which holds the die. The die comprises an integrated circuit, and the carrier holds the die in singulated form. Typically the die is placed in the carrier without any packaging which may protect the die. The identification code may be applied to the die before or after it is deposited into the carrier.

BRIEF DESCRIPTION OF THE DRAWINGS

The invention is further described by way example with reference to the accompanying drawings, wherein:

Figure 1A is a cross-sectional illustration of a carrier module of the present invention comprising a carrier supporting a die with a cover securing the die within the carrier.

Figures 1B and **1C** illustrate one particularly preferred embodiment of the invention.

Figure 1D illustrates another particularly preferred embodiment of the invention.

Figure 1E illustrates a JEDEC tray containing nine carriers, with a tenth oriented to be added to the tray.

Figure 2A is a top view of one embodiment of the carrier of the present invention.

Figure 2B is a top view of a second embodiment of the carrier of the present invention.

Figure 3A is a top view of one embodiment of a cover of the present invention having holes therein.

Figure 3B is a top view of a second embodiment of a cover of the present invention having holes therein.

Figure 4 is cross-sectional view of an alternative embodiment of the carrier module of the present invention comprising a carrier supporting die with a cover snap-locked to said carrier and securing said die within said carrier.

Figure 5 is a cross-sectional view of the embodiment of the present invention illustrated in **Figure 1A** mounted on a test board and using stand-offs.

Figure 6A is cross-sectional view of an alternative embodiment of the present invention mounted on a test board and using shims.

Figure 6B is a cross-sectional view of an alternative embodiment of the present invention mounted on a test board and using shims.

Figure 7 is a cross-sectional view of another embodiment of the present invention wherein the carrier has two ledges within each opening and the cover has an added component extending down into the opening to secure the die within the carrier.

Figure 8 is a cross-sectional view of an alternative embodiment of the present invention wherein the carrier itself secures the die in place through use of snap locks rather than a cover.

Figure 9A is a cross-sectional view illustrating a method of clamping the carrier module of the present invention to a board by lowering an arm across the back of the board.

Figure 9B is a cross-sectional view of another embodiment of the present invention wherein the carrier is secured to the load board by spring-loaded retaining arms.

Figure 9C is a cross-sectional view of another embodiment of the present invention wherein the carrier is secured to the load board by spring loaded, threaded bolts.

Figure 9D illustrates one particularly preferred embodiment of the invention.

Figure 10 is a cross-sectional view illustrating an alternative method of mounting the carrier module to the board, wherein the carrier module is mounted first on the arm and then lowered into place on the board.

Figure 11 is a cross-sectional view illustrating a method of mounting the carrier module illustrated in **Figure 8** to a board.

Figure 12A is a cross-sectional view of a carrier module of the present invention wherein the positioning holes on the board having a sloping front edge

such that the carrier module slides into place and creates a swiping action by the die's contact springs across the corresponding contact pad on the board.

Figures 12B and **12C** illustrate side and top views of a test board including springs, and a corresponding carrier, cover and die.

Figure 13A is a top view of a carrier of the present invention further comprising a tracking label on the carrier and an identification mark on the die.

Figure 13B is an end view of a carrier of the present invention further comprising a tracking label on the carrier and a connection to an electronic storage device.

Figure 13C is a perspective view showing a tray for multiple carriers.

Figure 14 is a flowchart illustrating the steps involved in tracking a carrier and/or singular die through manufacturing, transport, and final use.

Figure 15 is a flowchart illustrating the steps involved in fabricating and then utilizing the present invention.

DETAILED DESCRIPTION OF THE INVENTION

A method and apparatus for manipulating an integrated circuit (IC) die through testing and a final application is described. A method and apparatus for tracking the die is disclosed. In the following detailed description, numerous specific details are set forth in order to provide a more thorough understanding of the present invention. However, it will be obvious to one skilled in the art that the present invention may be practiced without these specific details. In other instances, well-known devices, methods, procedures, and individual components have not been described in detail so as not to unnecessarily obscure aspects of the present invention.

The present invention provides a carrier for use in transporting and tracking IC die through testing after they have been cut from the original wafer. The carrier of the present invention is generally used to transport and support the die during testing, and may be labeled to allow for the tracking of both the carrier and its individual components. The carrier of the present invention may be used with die having either soldered spring, pin-in-hole spring, or pressure spring contacts. Once testing is complete, the carrier may then be transported and mounted on a printed circuit board to form a final substrate package.

The carrier may be used with die having no springs at all, for interfacing with test or final application products that include suitable contact mechanisms for establishing electrical contact with the die. One preferred test product includes resilient, free-standing contact elements, much like the springs on silicon described in detail in this application. One preferred final application product includes similar springs.

A general embodiment of the present invention is illustrated in **Figure 1A**. The carrier, or lower component, 10 is used to support the die 12 during the transport, testing, and/or final application use of the die 12. The carrier 10 is

typically made of an organic material such as polymer and may be formed using injection molding. In one preferred embodiment, epoxy glass laminate material is cut to size and machined to a desired form. The die 12 is placed into the carrier 10 through the opening 14 where it resides on ledge 18 lining at least a portion of the base of the opening 14. Note the walls of opening 14 preferably are chamfered to allow for an easy insertion of the die 12 into the opening 14. Also, note that the die is placed into the carrier before packaging the die. That is, there is no package that surrounds and protects the die. After testing in the carrier 10, the carrier may serve as the final package for the die 12.

The spring components 16 of the die 12 extend downward through the opening 14 to allow for future electrical contact with the contact pads of either a test board, a printed circuit board, or a final application substrate package. The spring components 16 extend through the opening 14 past the lower side of the ledge 18. The spring components or contacts 16 are generally elongate resilient electrical contact elements. A detailed discussion of such resilient electrical contact elements is found in U.S. Patent No. 5,864,946, entitled "Method of Making Contact Tip Structures", issued February 2, 1999, to Eldridge et al., assigned to the assignee of the present invention, and is incorporated herein by reference.

Note that the height H = H1 – H2 provides the maximum compression limit for the spring components 16. H1 is the dimension from the bottom of carrier 10 to the bottom of cover 20, which is the location of the top of the die when the springs are under compression. H2 is the thickness of the die. Another factor to consider is that in certain geometries, the springs will contact terminals that are raised above some contact surface and thus come within the opening 14. In this instance, the thickness of the terminal must be considered in determining the minimum spring length under maximum compression.

In other words, the springs cannot be compressed more than the height H. In general, there are three spring component heights that are particularly noteworthy – 1) new product or resting height (e.g., 30 mils), 2) the burn-in height for testing (e.g., 28 mils), and 3) the operating height (e.g., 25 mils). It is preferred to compress the springs as little as possible during testing so as to preserve spring life, that is, to maintain resilience for best performance in later operation. In other words, increased compression of the spring components is desired for final operation to ensure a good electrical contact, and minimal compression before the final operation.

Figures 1B and **1C** illustrate exploded side and top views of the apparatus of **Figure 1A**. These show a 2 by 4 arrangement of die, with a cover 20 with corresponding openings. **Figure 1D** shows another preferred embodiment of the present invention. This shows a one by 8 arrangement of eight die, carrier 10, cover 20, and heat radiating elements 20A. In this exploded view, securing pins 8 are shown exaggerated in length to illustrate the exploded view. In practice, securing pins 8 would be of a length to hold cover 20 securely in place against carrier 10, with carrier 10 secured against board 30.

Figures 2A and **2B** illustrate top views of the carrier 10, showing two examples of possible arrangements of the openings 14 in the carrier 10. **Figure 2A** is an illustration of a carrier 10 (corresponding with the cross-sectional view of carrier 10 shown in **Figure 1A**) having eight openings arranged in two rows of four openings 14 each. **Figure 2B** is an alternate arrangement, wherein eight openings 14a are positioned in the carrier 10a (this top view does not directly correspond with the cross-sectional view of **Figure 1A**) in a single linear row. Note that although both **Figures 2A** and **2B** depict a carrier 10 having eight openings 14 arranged in a linear fashion, this is not a requirement of the invention. Instead, the actual

number, position, and orientation of the openings 14 in the carrier 10 is a design choice dependent on numerous factors.

Referring back to **Figure 1A**, a cover (or lid, etc.) 20 is coupled to the carrier 10. As with the carrier, the cover 20 may be formed from an organic material using injection materials. In one preferred embodiment, the cover is machined from epoxy glass laminate. The cover may also be comprised of a metallic sheet to assist in heat dissipation, and may have added heat dissipation components, such as fins, mounted thereon. The cover may be considered a retaining element. Note that any retaining element such as snap locks, ball bearings, retainers, a single bar, etc. may be used in addition to a cover to secure the die within the carrier. Such retaining elements will typically be positioned to mechanically abut a portion of a backside surface of the die when the die is placed in the carrier.

The cover 20 serves two primary functions. First, the cover 20 is used to secure the die 12 in the opening 14 of the carrier 10 during transport. Second, the cover 20 provides resistance against the backside of the die 12 when the die 12 is under compression during testing or use. This compression arises from the force of the springs pushing against the die 12 and the underlying substrate, such as test board 30 (see **Figure 5**). The cover 20 may be coupled to the carrier 10 in any one of several mechanical coupling regimes. Illustrated in **Figure 1A**, is snap shell 22B and snap head 22B. Snap head 22A is secured to cover 20 by rivet 22. However, a nut and bolt or a clamp can also be used. **Figures 5** and **6B** include an illustration of another alternative embodiment using a variation of a snap lock to secure the two components together. The method of coupling the carrier 10 and the cover 20 is not significant other than to ensure that it is a temporary connection, which is useful in most (but not all) instances of the invention. A temporary connection allows the cover 20 to be removed at some future time, for example to remove die 12 after

testing or use, or to allow a particular die 12 to be removed and replaced or to allow the cover 20 itself to be replaced.

The cover 20 also may comprise openings 24 that expose a portion of the backside of the die 12. In **Figure 1A**, a single opening 24 exposing the majority of the backside of the die 12 located such that it is approximately over the center of both the die 12 and carrier opening 14 is shown. **Figure 3A** provides a top view of the cover 20 showing the rectangular openings 24 positioned over each of the die 12. Note, however, that the openings 24 are not required to be either rectangular or singular over each die. For example, **Figure 3B** illustrates one possible alternative embodiment of the cover 20a, wherein there are two oval openings 24a over each of the die 12 in the carrier 10.

Although the cover 20 is not required to have openings and may be a solid sheet of material, the openings provide several advantages to the carrier of the present invention. First, the openings 24 allow a temperature-controlled gas to be delivered directly to the backside of the die 12. During burn-in testing, a temperature-controlled gas assists in maintaining a constant, desired temperature. Primarily, this allows the temperature of the die 12 to be modified so the performance can be evaluated at different operating temperatures. A hot gas could be delivered directly to the backside of the die 12 as needed for testing purposes. Second, the openings 24 allow additional couplings to be made to the die under test. For example, a thermocouple could be used to monitor the temperature of each die, or other couplings could be used to take measurements, such as resistance, during testing or operation. Third, the openings 24 provide access to the backside of each die 12 allowing an identification mark ID to be added as needed (see **Figure 13**). For example, the die 12 could be marked with an ink dot to indicate failure of the test. A part could be marked to show the results of testing, such as directly marking a speed grading. Product identification information such as the manufacturer, lot number

and the like can be applied. Additionally, a bar code or other machine readable code could be imprinted on the back of each die to allow for tracking of each die 12 or a magnetic strip with a code could be placed on the die. (See tracking discussion below for more detail.)

Referring back to **Figure 1A**, the snap used to couple the carrier 10 and cover 20 also serves to provide a stand off 26. In one preferred example, the stand off 26 is part of the fastener securing snap 22B to carrier 10. A stand off can be designed into or otherwise secured to housing 10.

The stand off 26 extends from the base of carrier 10 down lower than the spring components 16 and serves to provide protection for the spring components 16 during transfer, storage or handling. For example, if the carrier 10 were set down on a flat surface prior to testing, the stand off 26 would prevent the spring components 16 from being compressed. Note that if a method of coupling the carrier 10 and cover 20 other than a snap and rivet 22 as shown in **Figure 1A** is used, for example use of a screw that does not extend all the way through the two components or use of a snap lock, a stand off may be added to or fabricated as part of the carrier during the manufacturing process. **Figure 4** illustrates use of such a fabricated standoff to provide protection for the springs when using a snap lock to couple the carrier and cover.

The standoffs also provide a very significant second function by assisting in correctly positioning the carrier onto a board. During testing, the carrier 10 will be mounted on a test board 30 as shown in **Figure 5**. The spring components 16 will be placed into contact with contact pads 31 on the test board 30. When mounting the carrier 10 onto the test board 30, it is thus important to ensure that each spring component 16 is lined up with and in contact with a contact pad 31 on the board 30. To accomplish this, positioning holes 32 in the test board 30 are coordinated with the stand offs 26. In this manner, when the carrier 10 is mounted on the board 30

and the stand offs 26 reside within the positioning holes 32, the spring components 16 are in contact with the contact pads 31 on the upper surface of the board 30. In the case of the embodiment **of Figure 5**, a test board 30 may have holes 32 that are shallower than holes on a final substrate that is part of the final package of the die. In this way, the springs are compressed less in testing than in final use. As may be seen in **Figures 2A** and **2B**, in one preferred embodiment, three or more positioning holes and corresponding stand offs are used in such a manner as to allow only one correct alignment and fit. Note that although only three stand offs 26 are shown in **Figures 2A** and **2B**, more could easily be added as needed. In a particularly preferred embodiment, illustrated in **Figures 1B** and **1C**, two offset positioning holes are sufficient to align the pins. Alignment pins 13 are secured to bolster plate 13 on one side of board 30. Holes 15 in the carrier and cover are aligned with alignment pins 13. With a moderate offset, it is easy for an operator to align the carrier correctly. Although the carrier could be inserted on the opposing alignment pins, the carrier would be obviously off-alignment with the fixture, and thus it is easy to set the alignment correctly.

Figure 1E shows a standard JEDEC tray with 9 carriers in slots and one slot open. A carrier 10 is shown ready to insert into the tray.

Although the use of stand offs is preferred, the present invention is not limited to use with stand offs. For example, as shown in **Figure 6A** and **6B**, shims 60 may be used to prevent the spring components from being compressed to the maximum limit. The shims may be used during testing but not during use of the die to compress the springs less during testing than use. When using the shims 60 instead of stand offs, alternative means are required to assist in the positioning and lining up of the carrier when mounted on the board. For example, standard alignment techniques such as split beam optics can be used to identify the positions of the springs and the terminals and to bring them together in precise alignment.

A second embodiment of the present invention is illustrated in **Figure 7**. In this second embodiment, the carrier 70 has both a first ledge 72 and a second ledge 74 lining opening 76. The die 12 is lowered through the opening 76 and is supported by the first ledge 72. The cover 78 has an extended component 79 that fits down into opening 76 and resides against the second ledge 74. In this manner, the component 79 serves to secure the die 12 in the carrier 70 and provides resistance to the compressive force exerted against the spring contacts of the die 12. Note, however, that this embodiment could be further modified such that an actual second ledge was not required and instead the extended component 79 would reside against the back surface of the die 12. In one embodiment of the invention, different corners having extended components with different heights may be used to cause the springs to be compressed less in testing than in use.

A third embodiment of the present invention is illustrated in **Figure 8**. **Figure 8** illustrates a carrying apparatus having merely a carrier with no cover. Instead, the carrier 80 has spring locks 82 that secure the die 12 within the opening 84. The spring locks are a form of a retainer that is coupled to the carrier. As the die 12 is lowered into the opening 84, the spring locks widen to allow the die 12 to pass through. Once the die 12 is completely lowered into the opening 84, the spring locks 82 return to their original position and lock the die 12 into place. The spring locks can be held in an "open" position by handling equipment to allow easy passage of a die into the carrier, then moved to a "closed" position to maintain the die in place. This embodiment of the present invention is advantageous in that it eliminates several parts and steps of the manufacturing process. However, because the backside of the die 12 is not fully supported, when a compressive force is exerted, the silicon die 12 may be subject to warpage and damage. The specific selection of test die, dimensions of the die, spring forces, strength of materials and the like will influence the suitability of this design for a given application.

Once each of the different embodiments has been positioned on the board, the carrier module (comprising the carrier, die, and cover) must be securely coupled to the board. This coupling can be achieved in any one of several ways. In many preferred embodiments, the coupling is not permanent so that the carrier module may be released and removed. Note that both individual and multiple carriers may be mounted on a board.

One preferred embodiment for coupling the carrier module to the board, is a clamshell such as the one depicted in **Figure 9A**. A support 90 resides at one edge of the board. A hinged arm 92 extends from the support 90 and across the backside of the carrier module 94. Once the carrier module has been positioned on the board 30, the arm 92 is lowered such that it lays across the back of the carrier module 94. Once the arm 92 is lowered, it snaps into place with a second support arm 96 on an opposite side of the carrier module 94 that has a receiving snap lock 98 that then holds the arm 92 secure. The size of the arm 92 relative to the carrier module 94 and the number of such arms used is purely a design decision dependent primarily on the size of the carrier module 94. As just one example, an arm 92 may secure a single carrier module 94 wile a different arm 92 may secure several carrier modules.

Referring to **Figure 9B**, a hinged cover secures a die in position against a load board. Housing 91 includes an opening for die 12, very much like the structure of the carrier discussed in detail above, for example in connection with **Figure 7**. Top 92A is hinged to rotate and connect to housing 91. In the open position, it is easy to insert die 12. In the closed position, it serves to secure die 12. It may be secured in the closed position by latch 93. Housing 92 may be affixed to board 30 in a permanent or semi-permanent manner, as by screws from the opposite side of board 30 (not shown). This is particularly useful for testing limited quantities of die, as during early research phases.

Figure 9C illustrates another method of securing the carrier to the board. Each post 90B supports an arm 92B, which pivots against the carrier to secure it to the board 30. Arm 92B is under tension from torsion spring (not shown), which maintains pressure against the carrier. The spring force is sufficient to keep the carrier in position, but can be overcome by an operator positioning the carrier on the board.

As shown in **Figure 10**, it is clear that the carrier module 104 does not first have to be positioned/mounted on the board 30. Instead, in one embodiment, the carrier module 104 may be mounted on the arm 102 itself (again by some non-permanent mechanical means) and then lowered until the carrier module 104 is in the correct position relative to the board 30 and the arm 102 is snapped into place and held secure by the snap lock 108 of the second support 106.

A modification on the above design may be used with the third embodiment discussed above and shown in **Figure 8** (i.e., a carrier using snap locks to secure the die rather than a cover). **Figure 11** shows an arm 112 having extending components 115 that fit into the opening 84. These extending components 115 provide the support and resistance required when the die is under compression that will prevent the die from becoming damaged due to warpage. As with the previous clamshells, the arm 112 is lowered until it snaps into place and is held secure by the snap lock 118 of the second support 116.

Another feature that may be incorporated in the various embodiments of the present invention allows the spring contacts to have a wiping action across the landing (or contact) pads as the carrier module is mounted on the test board. When making any connection between two electrical components, it is often advantageous to move one relative to another so that one makes sliding contact with the other. This tends to dislodge debris that might inhibit a good electrical connection. Thus,

the ability to allow a wiping action with soldered springs during testing is a significant benefit.

During testing, a wiping action is typically inherently provided by a spring pressure connection, but not necessarily by springs for solder connection. Preferred spring shapes for pressure-connect springs include a geometry such that compression of the spring directly towards the supporting substrate (in the Z axis if the substrate is in the XY plane) causes the contact region of the spring to move laterally, that is, with an XY component. This leads to a wiping action across the face of a terminal, which typically is more or less planar. Preferred spring shapes for solder-connect springs or springs for pin-in-hole connection may not have much or any XY movement upon compression.

One method of achieving a wiping action is illustrated in **Figure 12A**. In this embodiment, the positioning holes 122 on the board 120 are modified slightly such that they have a sloping front edge 124. When the carrier module 126 is placed over the front edge 124 of the position holes 122 and lowered into position, the stand offs 128 slide down the sloping front edge 124 before coming to a secure rest in positioning hole 124. This sliding motion of the carrier module 126 causes the contact springs to wipe across the contact pads on the board 120. The wiping action results in a better final electrical connection between the contact springs and the contact pads.

An alternative embodiment (not shown) has a different positioning hole, with a pattern substantially in the plane of the board that allows for translation of the carrier relative to the board. As the carrier is brought into contact with the board, the carrier is moved within the positioning hole to create a wiping action. When using a handler to position the carriers, it is straightforward to program a lateral motion as part of the loading process.

Thus far, the discussion has centered on carriers for die where the die include springs. However, the same principles apply well to an apparatus and method where the test board, or a final packaging apparatus includes springed elements. Referring to **Figures 12B** and **12C**, and comparing **Figures 1B** and **1C**, load board 30A can be prepared with springs. One preferred way to position springs on such a board is described in detail in United States Patent 5,772,451, entitled "Sockets for Electronic Components and Methods of Connecting to Electronic Components". That patent describes securing resilient contacts to a suitable substrate. The substrate can include contact such as solder balls opposite the springs, and in turn can be reflowed to connect to terminals on a substrate such as a printed circuit board. Using such component here, a substrate 125 can be prepared with springs 127 and positioned to contact terminals on semiconductor die as shown. One embodiment positions solder balls 123 on the side of the substrate 125 opposite the springs 127. The solder balls can be secured to terminals on the board, for example by reflowing. The springs can be brought into contact with die for testing or other operation of the die. When desired, a substrate 125 can be removed from the board for replacement, repair, or other purposes. Standoffs 26 are increased in height to set the correct spring tension during test. Correspondingly, if a similar carrier is to be used in final products, a springs connection such as that illustrated in **Figure 12B**, can be provided, with suitable stand offs for proper connection.

The die can be placed in the carrier and managed as described in this disclosure generally. In this way, conventional die without springs can be manipulated, tested and used in very much the same ways as described above for die with springs.

The present invention may be further improved upon through use of a tracking device. As shown in **Figure 13A**, for example, a tracking mechanism may be added to the carrier 130. Optionally, an identification mark ID may be applied to

the backside of the die 12 residing within the carrier 130. The ability to track a carrier and know at any given time the history of the die supported therein provides several advantages over the prior art. By placing a tracking label on the carrier and recording information concerning each die added to and/or removed from the carrier, at any given time a user can access the information on the die, including the particular wafer it came from and the specific manufacturing lot of wafers which included even the specific manufacturer. Although tracking abilities exist on the wafer level, no such ability is currently available on a die level. However, by placing a tracking label on the carrier of the present invention, information on the die level may be maintained.

As shown in **Figure 13B**, the tracking label may advantageously be placed on the side of the carrier so it is visible even when a cover is in place. In addition, as just one alternative method, the carrier may be fitted with a programmable device such as a EEPROM. Connections to a EEPROM are illustrated in **Figure 13B**.

First, a tracking label or identification code is applied to the carrier (see **Figure 14** for flowchart). Note, however, that the tracking label may be applied to the carrier after the carrier is loaded with die. The wafer is diced. As each die is loaded into the carrier, information concerning that die is stored in a tracking label on the carrier. The information may include, but is not limited to, information identifying the specific wafer from which the die was created, information identifying a specific semiconductor wafer in a specific lot of wafers, information identifying a particular wafer processing lot in which the wafer was created, and the location of the die on the wafer. The tracking label may comprise a bar code or a code stored in a memory device, such as a magnetic media or a semiconductor memory device, on the carrier.

This process is even more powerful in a particularly preferred embodiment. Wafer probing is performed as usual. Parts failing even basic testing are noted. For devices that are amenable to modification, the parts may be modified at this time.

For example, many memory devices are manufactured with redundant sub-units. Preliminary testing identifies sub-units that are passing or failing and automated equipment can select an appropriate group of functional units so the device as a whole will function properly. Any amount of information can be tracked on these parts, from merely noting the failures to elaborate records on which units of which devices were found functional, and any other information that might be useful to manufacturing. As just one more example, in many manufacturing situations, test elements are fabricated in otherwise-unused portions of a semiconductor wafer. Such regions include scribe line regions, or unused portions near the edge of a wafer. Information about these test units can be maintained in a database together with information about devices found on the wafer.

The wide variety of process steps in the manufacture of semiconductors are likely to have some degree of variance in various regions of a wafer. Extreme care is take to minimize such variations, but to some extent parts in different regions of a wafer are likely to be slightly different. By tracking the identity of individual die as they are separated from the wafer and subjected to testing and other use, a wafer map can be reconstructed showing results of any desired test for a given die as well as its neighbors for any region of a wafer. Variations over lots of wafers can be detected and evaluated as well. Heretofore, such tracking has been at best extremely difficult as the identity of parts simply becomes too hard to monitor in a complex, high volume manufacturing environment.

This information can be extremely valuable for running a process in the fab. The information gleaned from testing is made available to the manufacturing floor as soon as practicable. In an automated system, thresholds can be established that trigger alarms for processes going out of specification, and the factory floor can be notified immediately. There are at least two major benefits in this feedback system when using the current system. First, since the wafers can be tested almost

immediately after dicing, there is minimal delay from release from manufacturing to achieving first test results. This can be in only hours, although it often will be a small number of days, but this is compared to a minimum of several days and typically several weeks using current processes. The second big advantage is that by tracking the identity of each die, a wafer map can be reconstructed. Where test results show any sort of variation that is related to a position on the wafer, this information can be very valuable to the manufacturing floor in being certain that processes are consistent in all regions of the wafer during manufacturing. The rapid time response (quick feedback loop) is particularly valuable here in that early samples of a run can be evaluated and later lots of the same run can be modified where appropriate.

Turning to the preferred embodiment, after testing and initial device repair, automated equipment dices the wafer. Handling equipment places selected die into a carrier. Information about the specific location of a specific die on a specific wafer is tracked, as in a manufacturing database. For example, a group of eight die can be loaded into the carrier of **Figure 2A**. By tracking the unique positions within the carrier, it is sufficient for the manufacturing database to track the carrier ID information, and the position of each die within the carrier.

The carrier can be marked in many ways, as noted above. One particularly preferred marking has a bar code or other machine readable code printed along the side of the carrier, in a position that can be read by automated handling and by operators even when a cover is over the carrier. Another particularly preferred marking includes a EEPROM device in the carrier. Automatic handling equipment can enter key information into the EEPROM. The equipment also can read information from the EEPROM. This might be as simple as a unique identification code, tied to the manufacturing database.

Groups of carriers can be positioned in a tray. A tray can be marked in much the same way as the carriers. Higher order organization is quite practical, as in organizing groups of trays in a cart. Depending on the number of die in a carrier, and the size of parts, a wafer may be singulated into die which fill carriers in some small number of trays, for example on the order of 5 to 10. Depending on the size of a production run, a lot of, for example, 25 wafers, then would occupy some 125 to 250 trays.

Referring to **Figure 13C**, tray 130 may be fitted with a series of grooves 131, each of which can accommodate a carrier. A front edge of tray 130 includes label 132. The tray supports programmable device 134, suitably an EEPROM, with connection 133 readily accessible for contact by automatic handling equipment. Thus the label can be a guide for human operators, and machine-scannable, if desired. The programmable connection can allow access to an electronic tracking device.

An identification mark may also be applied to each die itself. Typically, such an identification mark would be applied to the backside of the die (the side opposite the spring contacts) after it was loaded into the carrier, wherein the mark was applied through an opening in the carrier or may be applied before the die is placed into the carrier. The identification mark on the die may comprise an ink dot indicating success or failure of a testing sequence, a unique or semi-unique identification number, a bar code retaining more specific information concerning the history of that particular die, or other useful information. As just one example, a series of die in a lot can be labeled with sequential, unique identification information. A separate lot may use the same identification information, but can be distinguished from the first lot by other means, such as time in the factory, some position in an external carrier, and the like. As a particular example, 16 bits of information may be used to track die within a lot, and some number of higher order bits might be used to identify larger groups of products.

The apparatus of the present invention may be compiled and used in a variety of manners (see flowchart of **Figure 15** for one example). For example, die may be loaded into a carrier and secured within the carrier by a retaining element to form a carrier module. This carrier module may then be positioned on a board and then secured down, for example by a clamp. Alternatively, the carrier module may be mounted on the clamp or coupling mechanism and then positioned on the board as it is secured/locked into place. Or, the carrier could first be mounted on the board and the die subsequently loaded and secured therein. Other variations on the steps followed in the compilation of the carrier module and its mounting on either a test board or a final substrate package exist. It is not required by the present invention, that a particular sequence of steps be followed in the compilation of the present invention.

CLAIMS

We claim:

1. A method for processing at least one die which comprises an integrated circuit, said method comprising:

applying an identification code to a carrier;

depositing a singulated die into said carrier, said singulated die comprising an integrated circuit, said carrier holding said singulated die.

2. A method as in claim 1 wherein said singulated die is deposited into said carrier without any packaging of said singulated die.

3. A method as in claim 1 wherein said identification code comprises information identifying at least one semiconductor wafer in a specific lot of wafers.

4. A method as in claim 3 wherein said identification code comprises at least one of a bar code or a code stored in a memory device on said carrier.

5. A method as in claim 4 wherein said memory device comprises one of a magnetic media or a semiconductor memory device.

6. A method as in claim 1 further comprising:

applying a die identification code to said singulated die, said die identification code comprising information relating to said die.

7. A method as in claim 6 wherein said die identification code comprises information identifying the wafer from which said singulated die was created.

8. A method as in claim 7 wherein said die identification code is applied to said singulated die after said singulated die is deposited into and secured in said carrier.

9. A method as in claim 7 wherein said die identification code further comprises information identifying a particular wafer processing lot in which the wafer was created.

10. A method as in claim 8 wherein said die identification code is applied to said singulated die through an opening in said carrier.

11. A method as in claim 1 wherein said carrier secures said singulated die during a burn-in testing of said singulated die.

12. A method as in claim 11 wherein said carrier secures said singulated die during use of said singulated die after said burn-in testing and said carrier acts as a final package for said singulated die.

13. A method as in claim 12 wherein said carrier secures a plurality of singulated dies comprising said singulated die.

14. A method as in claim 1 further comprising:

mounting a plurality of elongate, resilient electrical contact elements on contact pads of said singulated die.

15. A method as in claim 14 wherein said plurality of elongate, resilient electrical contact elements are mounted prior to depositing said singulated die into said carrier.

16. A method as in claim 15 further comprising:
applying a top on said carrier after depositing said singulated die into said carrier.

17. A method as in claim 15 further comprising:
mounting said carrier onto a substrate having a plurality of electrical contact pads.

18. A method as in claim 17 wherein said carrier is mounted on said substrate prior to depositing said singulated die onto said carrier.

19. A method as in claim 18 wherein said carrier is mounted on said substrate after depositing said singulated die onto said carrier.

20. A method as in claim 17 wherein each of said contact pads on said singulated die are electrically coupled to a corresponding one of said plurality of electrical contact pads on said substrate through a corresponding one of said elongate, resilient electrical contact elements.

21. A method as in claim 20 wherein each of said elongate, resilient electrical contact elements is freestanding.

22. A method as in claim 14 wherein each of said elongate, resilient electrical contact elements is freestanding.

23. A method as in claim 17 wherein said substrate is a test printed circuit board which is used to test said singulated die.

24. A method as in claim 17 wherein said substrate is a final package unit for said singulated die.

25. A method as in claim 17 wherein said substrate is used to test said singulated die, and if said singulated die passes testing, said substrate is used to package said singulated die for use.

26. A method as in claim 25 wherein if said singulated die fails testing, said singulated die is removed from said carrier and another singulated die is deposited into said carrier.

27. A method as in claim 2 wherein said identification code comprises information identifying at least one semiconductor wafer in a specific processing lot of wafers and wherein said method further comprises:

exposing said singulated die, while secured in said carrier, to a burn-in testing environment;

characterizing said singulated die based on said exposing;

reading said identification code.

28. A method as in claim 27 wherein said reading occurs after said characterizing and wherein said reading identifies said specific processing lot.

29. A method as in claim 27 further comprising:

mounting, prior to said exposing, a plurality of elongate, resilient electrical contact elements on contact pads of said singulated die;

mounting, prior to said exposing, said carrier onto a substrate having a plurality of electrical contact pads, wherein each of said contact pads on said singulated die are electrically coupled to a corresponding one of said plurality of electrical contact pads on said substrate through a corresponding one of said elongate, resilient electrical contact elements.

30. A method as in claim 29 wherein each of said elongate, resilient electrical contact elements is freestanding.

31. A method as in claim 29 wherein each of said elongate, resilient electrical contact elements is compressed less during said exposing than during final use of said singulated die.

32. A method as in claim 20 wherein each of said elongate, resilient electrical contact elements is compressed less during said exposing than during final use of said singulated die.

33. A method as in claim 20 further comprising removing said singulated die from said carrier after testing said singulated die and packaging said singulated die for use.

34. A method for processing at least one die which comprises an integrated circuit, said method comprising:

applying an identification code to a die;

depositing said die into said carrier, said die comprising an integrated circuit, said carrier holding said die in a singulated form.

35. A method as in claim 34 wherein said die is deposited into said carrier without any packaging of said die.

36. A method as in claim 34 wherein said identification code comprises information identifying at least one semiconductor wafer in a specific lot of wafers.

37. A method as in claim 36 wherein said identification code comprises at least one of a bar code or a code stored in a memory device on said carrier.

38. A method as in claim 37 wherein said memory device comprises a magnetic media.

39. A method as in claim 36 wherein said identification code comprises information identifying the wafer from which said die was created.

40. A method as in claim 39 wherein said identification code is applied to said die after said die is deposited into and secured in said carrier.

41. A method as in claim 39 wherein said identification code further comprises information identifying a particular wafer processing lot in which the wafer was created and said identification code is applied before said die is singulated.

42. A method as in claim 40 wherein said identification code is applied to said die through an opening in said carrier.

43. A method as in claim 34 wherein said carrier secures said die during a burn-in testing of said die.

44. A method as in claim 43 wherein said carrier secures said die during use of said die after said burn-in testing and said carrier acts as a final package for said die.

45. A method as in claim 44 wherein said carrier secures a plurality of singulated dies comprising said die.

46. A method as in claim 34 further comprising:

mounting a plurality of elongate, resilient electrical contact elements on contact pads of said die.

47. A method as in claim 46 wherein said plurality of elongate, resilient electrical contact elements are mounted prior to depositing said die into said carrier.

48. A method as in claim 47 further comprising:

applying a top on said carrier after depositing said die into said carrier.

49. A method as in claim 47 further comprising:

mounting said carrier onto a substrate having a plurality of electrical contact pads.

50. A method as in claim 49 wherein said carrier is mounted on said substrate prior to depositing said die onto said carrier.

51. A method as in claim 50 wherein said carrier is mounted on said substrate after depositing said die onto said carrier.

52. A method as in claim 49 wherein each of said contact pads on said die are electrically coupled to a corresponding one of said plurality of electrical contact pads on said substrate through a corresponding one of said elongate, resilient electrical contact elements.

53. A method as in claim 52 wherein each of said elongate, resilient electrical contact elements is freestanding.

54. A method as in claim 46 wherein each of said elongate, resilient electrical contact elements is freestanding.

55. A method as in claim 49 wherein said substrate is a test printed circuit board which is used to test said die.

56. A method as in claim 49 wherein said substrate is a final package unit for said die.

57. A method as in claim 49 wherein said substrate is used to test said die, and if said die passes testing, said substrate is used to package said die for use.

58. A method as in claim 57 wherein if said die fails testing, said die is removed from said carrier and another singulated die is deposited into said carrier.

59. A method as in claim 35 wherein said identification code comprises information identifying at least one semiconductor wafer in a specific processing lot of wafers and wherein said method further comprises:

exposing said die, while secured in said carrier, to a burn-in testing environment;

characterizing said die based on said exposing;

reading said identification code.

60. A method as in claim 59 wherein said reading occurs after said characterizing and wherein said reading identifies said specific processing lot.

61. A method as in claim 59 further comprising:

mounting, prior to said exposing, a plurality of elongate, resilient electrical contact elements on contact pads of said die;

mounting, prior to said exposing, said carrier onto a substrate having a plurality of electrical contact pads, wherein each of said contact pads on said die are electrically coupled to a corresponding one of said plurality of electrical contact pads on said substrate through a corresponding one of said elongate, resilient electrical contact elements.

62. A method as in claim 61 wherein each of said elongate, resilient electrical contact elements is freestanding.

63. A method as in claim 61 wherein each of said elongate, resilient electrical contact elements is compressed less during said exposing than during final use of said die.

64. A method as in claim 52 wherein each of said elongate, resilient electrical contact elements is compressed less during said exposing than during final use of said die.

65. A method as in claim 52 further comprising removing said die from said carrier after testing said die and packaging said die for use.

ABSTRACT

Methods for processing at least one die which comprises an integrated circuit. In one example of a method of the invention, an identification code is applied to a carrier. A singulated die is deposited into the carrier which holds the singulated die. The singulated die comprises an integrated circuit. The identification code may be applied to the carrier before or after depositing the singulated die into the carrier. The carrier may be used in testing the singulated die and may include a plurality of singulated die or just one singulated die. In another example of a method of the invention, an identification code is applied to a die. The die is deposited into a carrier which holds the die. The die comprises an integrated circuit, and the carrier holds the die in singulated form. Typically the die is placed in the carrier without any packaging which may protect the die. The identification code may be applied to the die before or after it is deposited into the carrier.

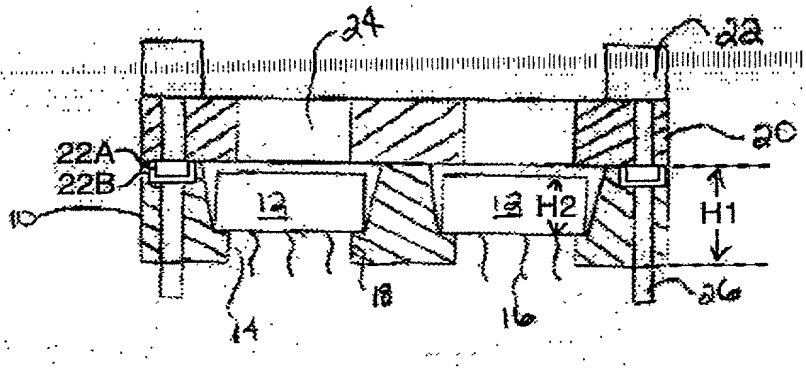


Figure 1A

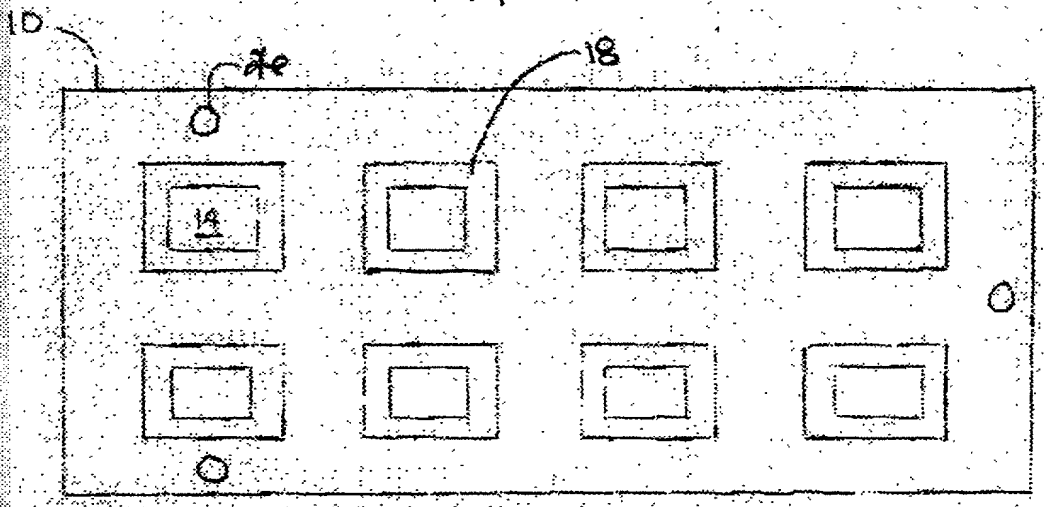


Figure 2A

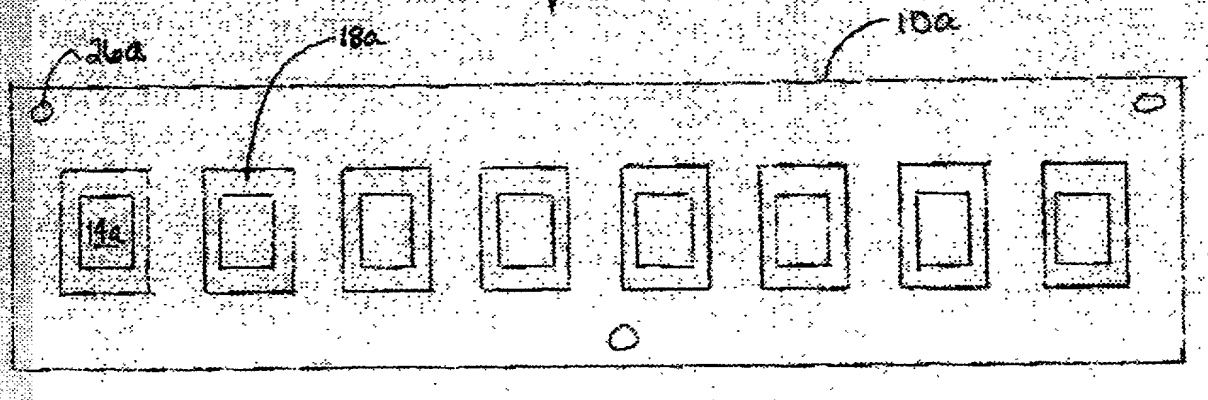


Figure 2B

Figure 1B

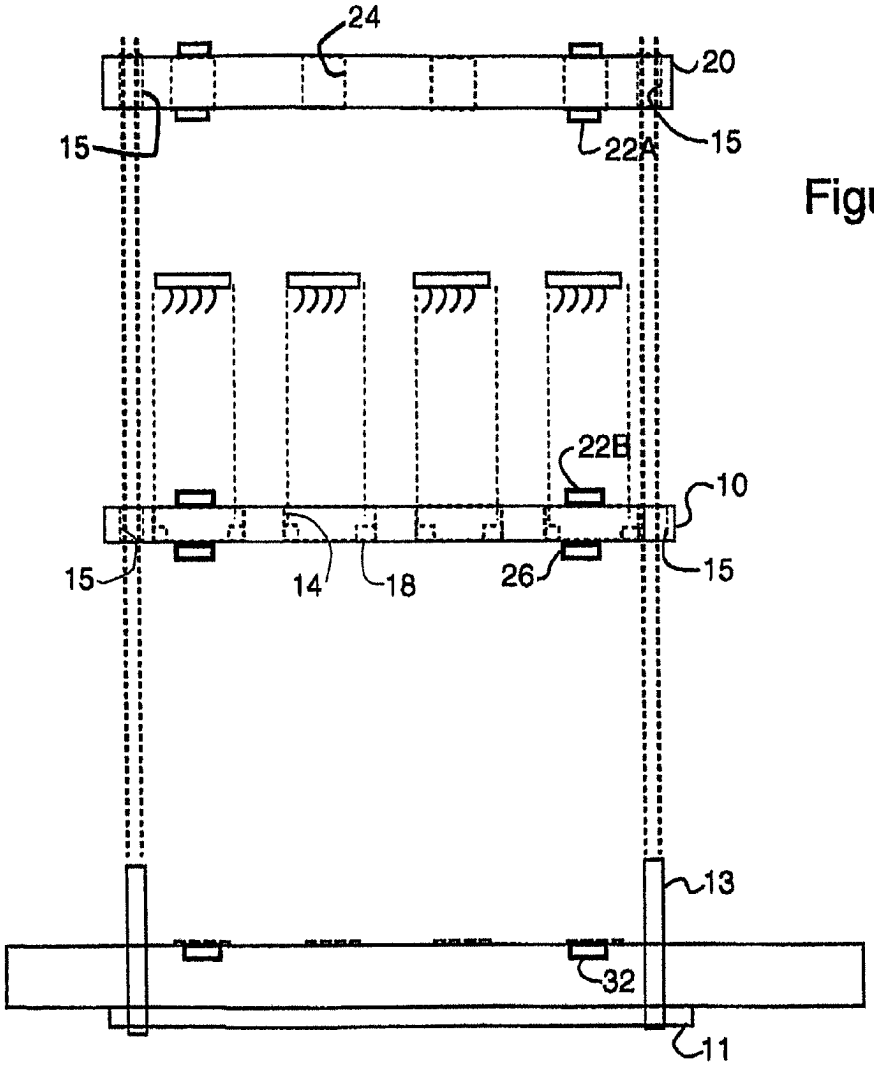


Figure 1C

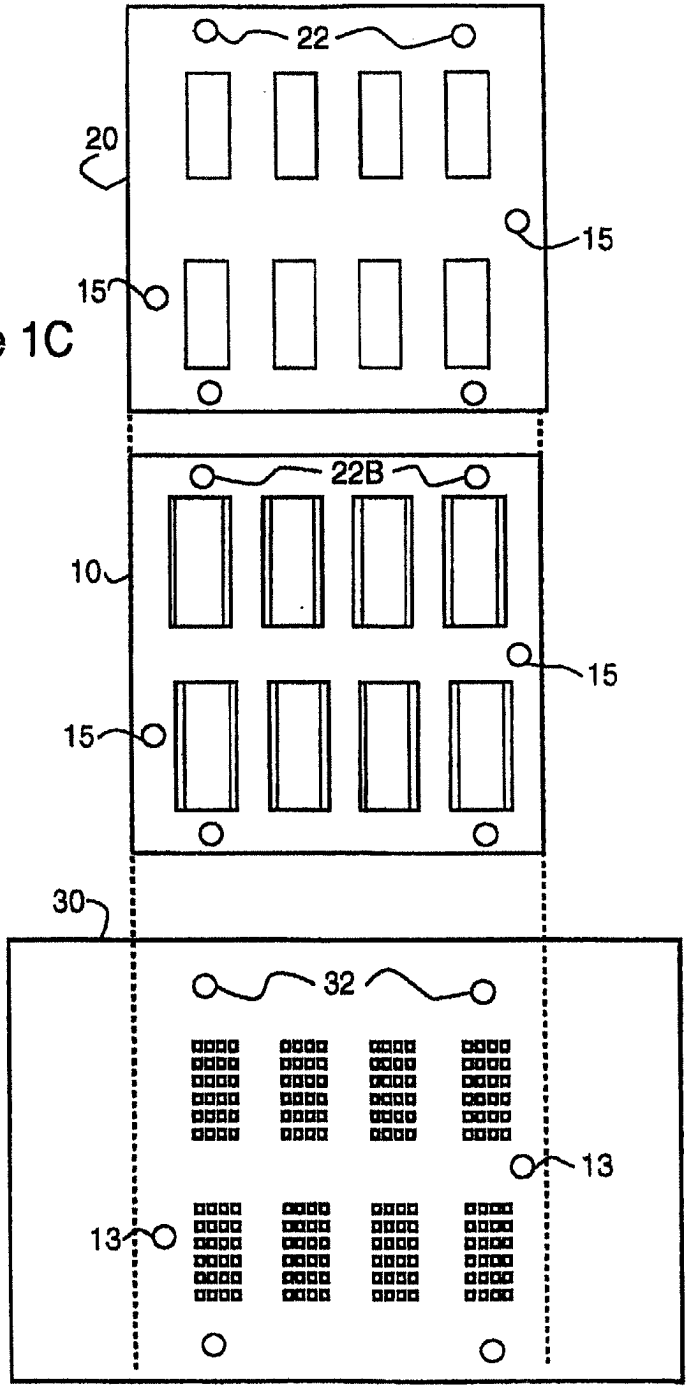
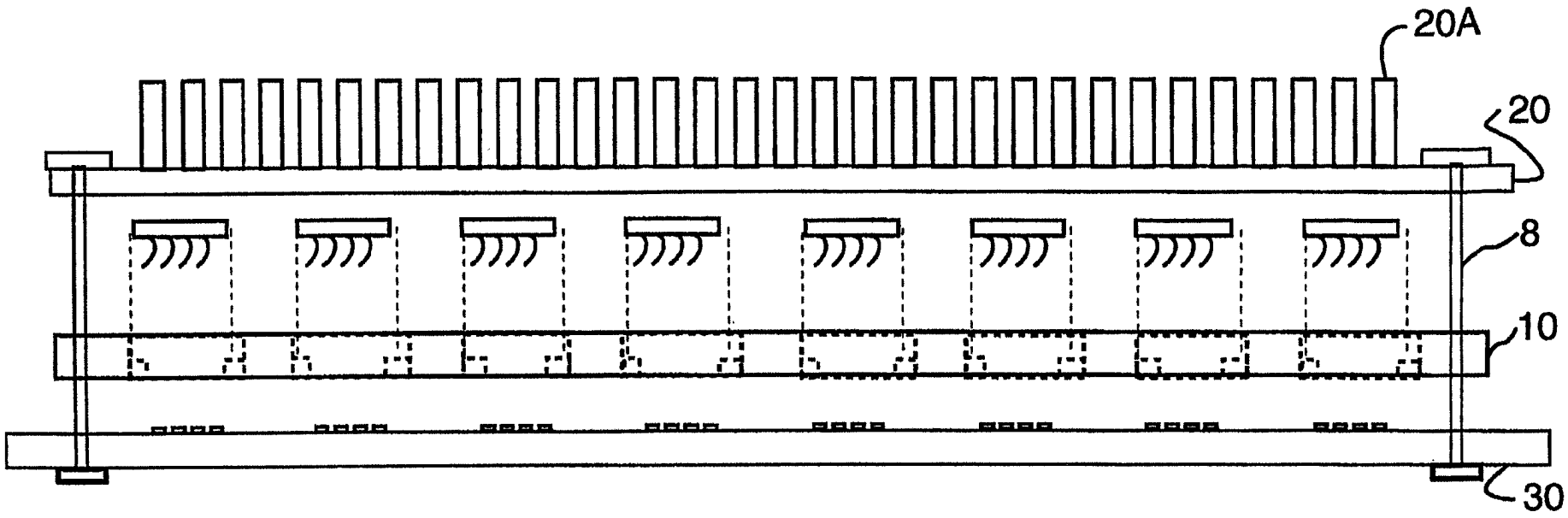


Figure 1D



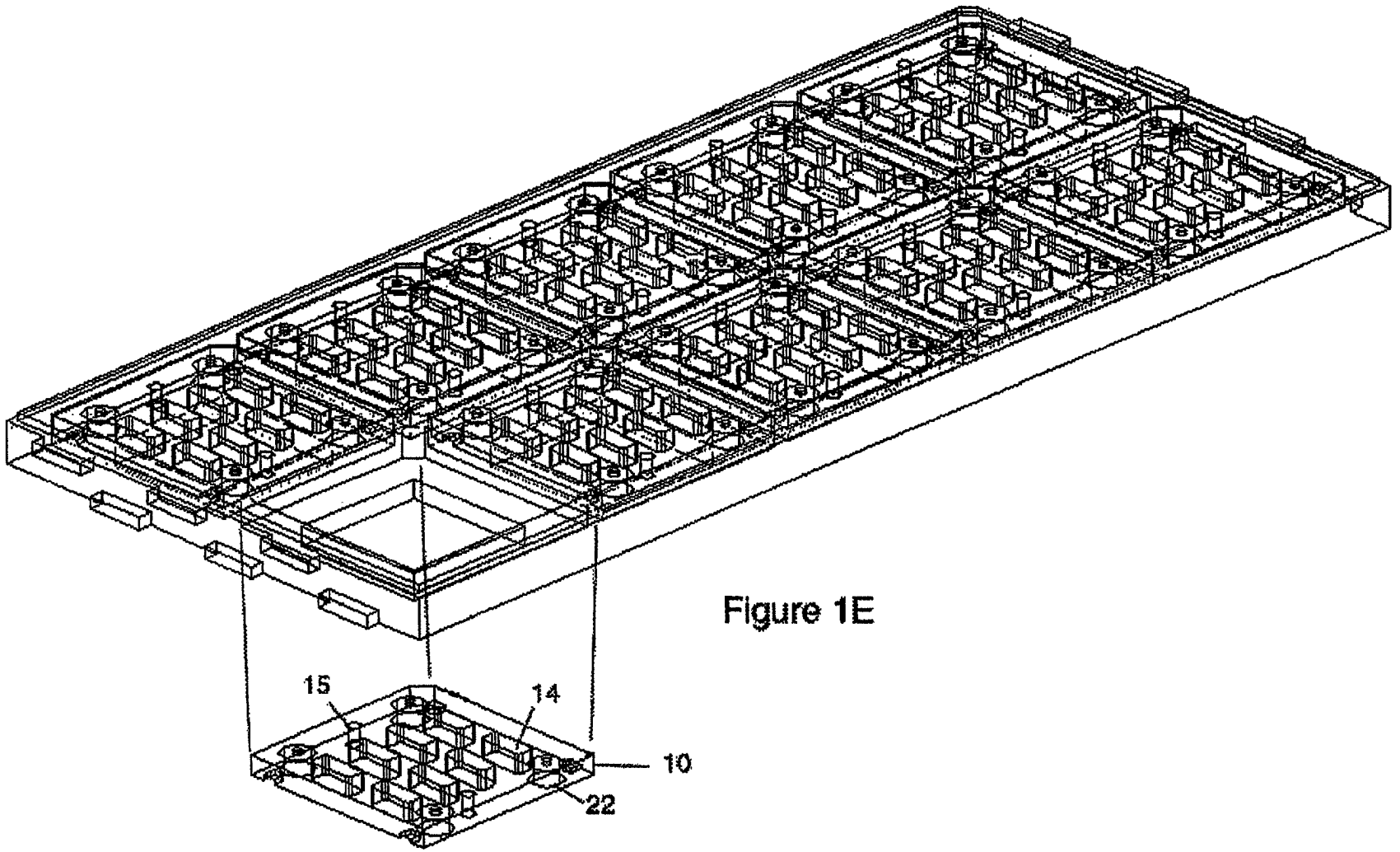


Figure 1E

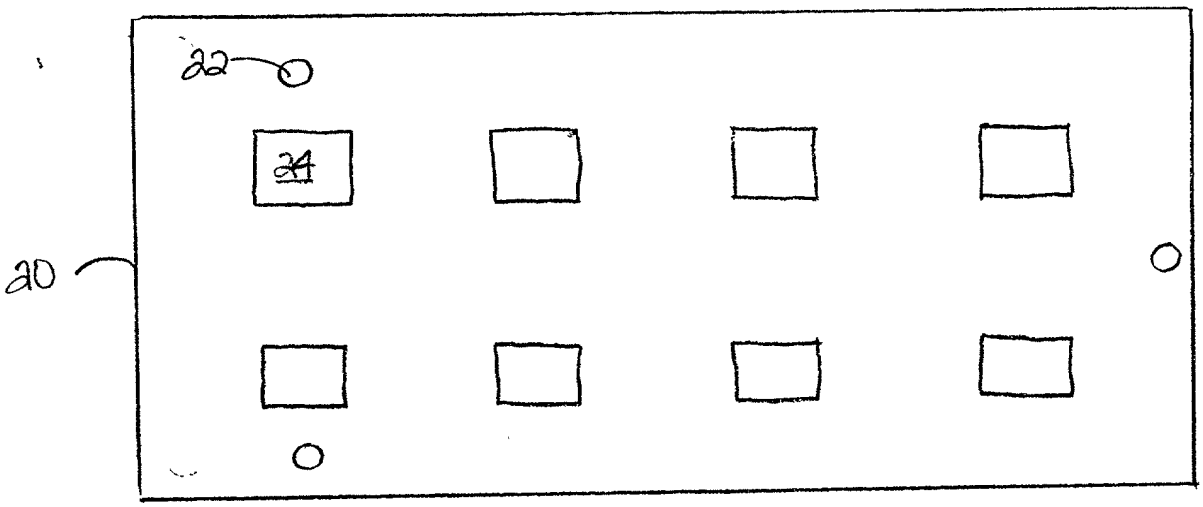


Figure 3A

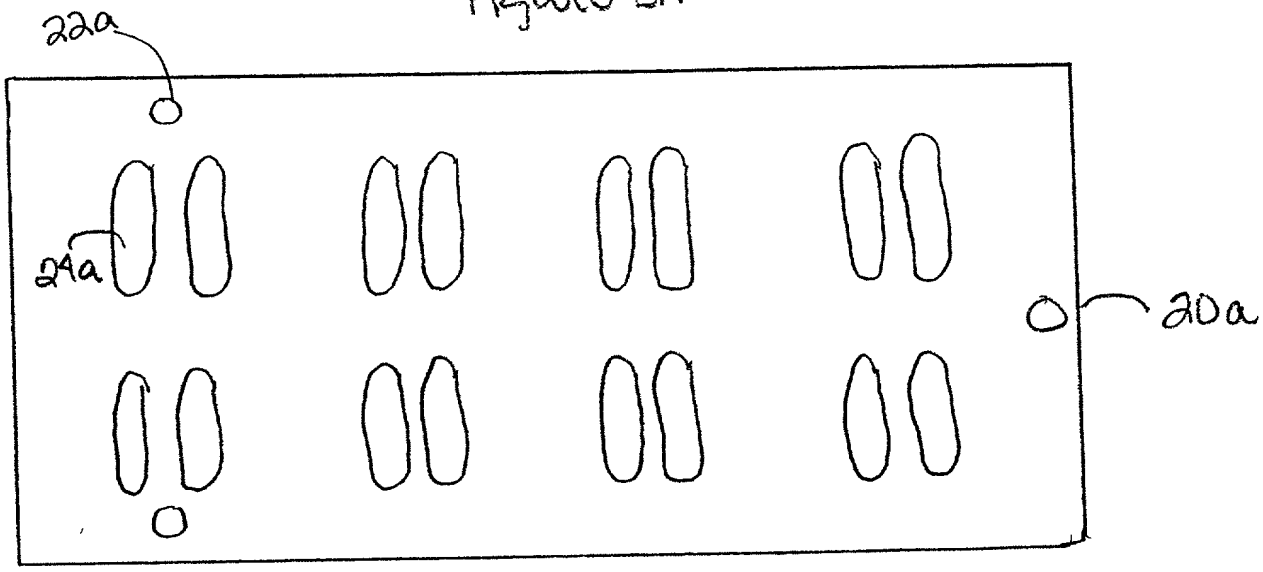


Figure 3B

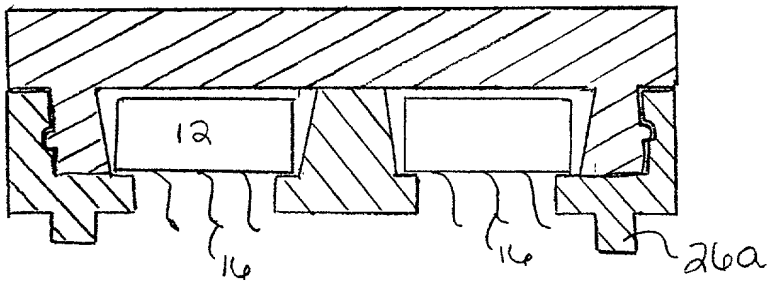


Figure 4

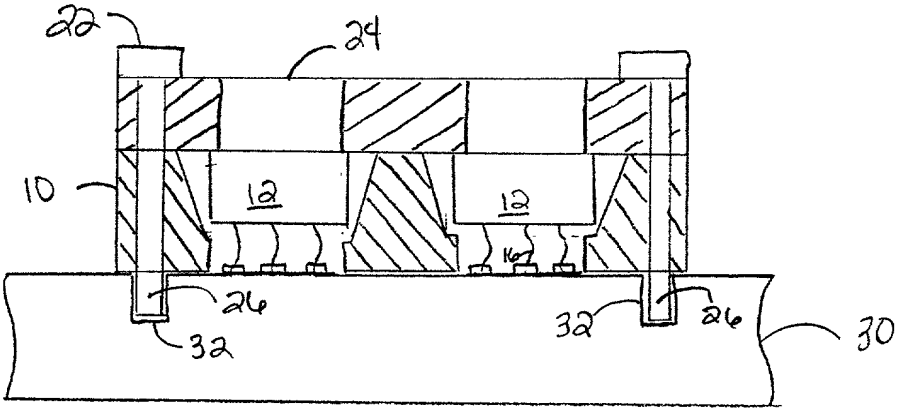


Figure 5

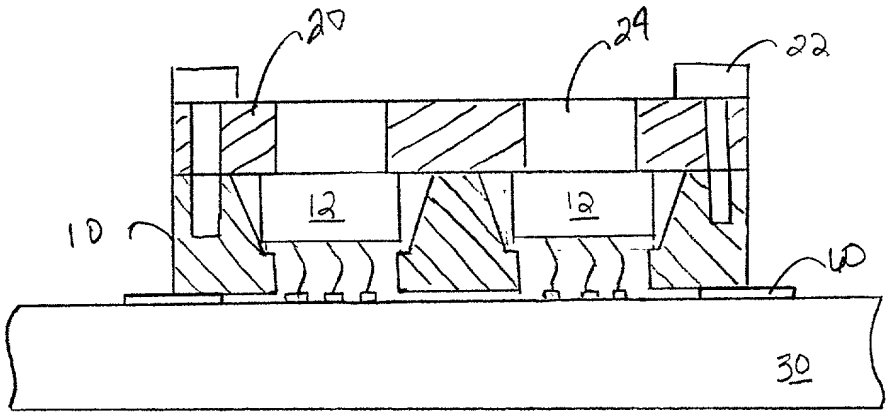


Figure 6A

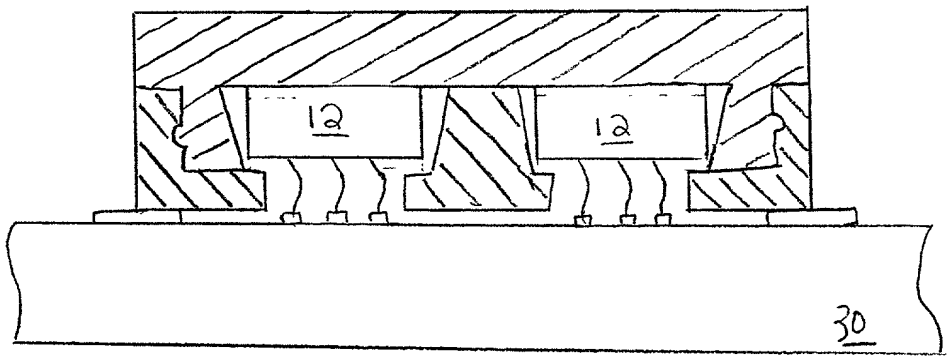


Figure 6B

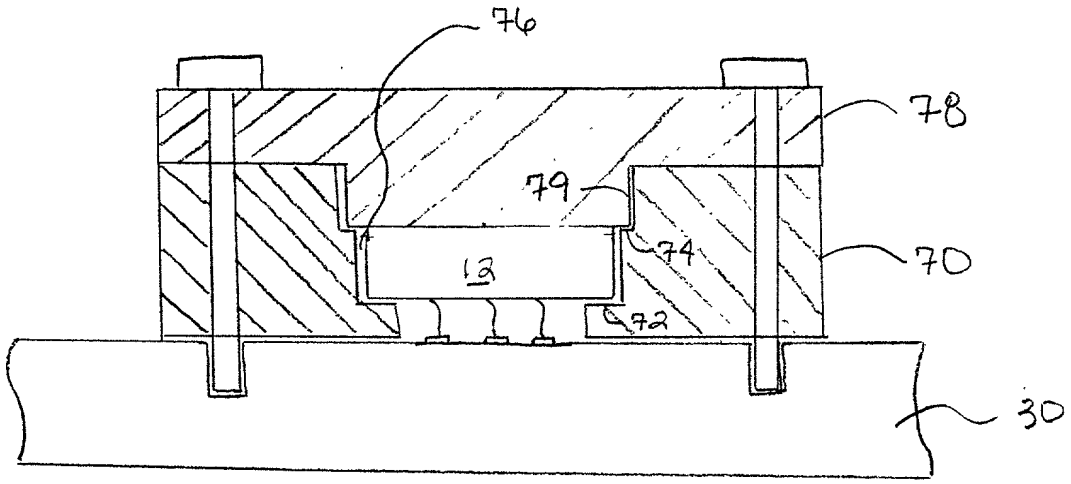


Figure 7

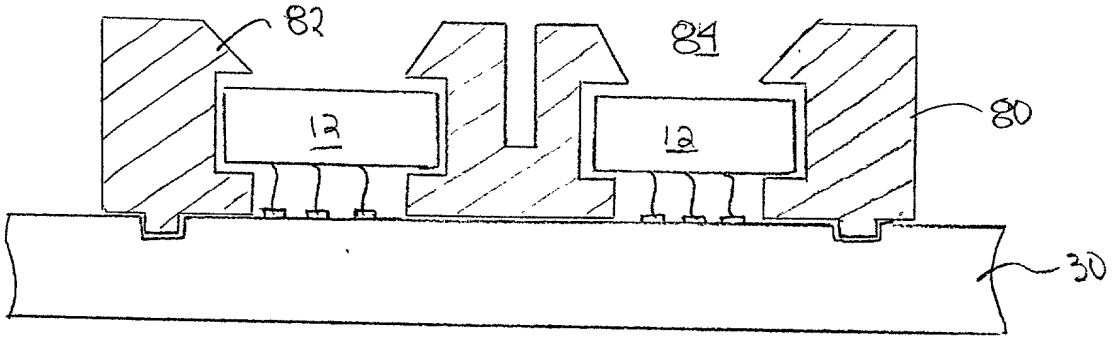


Figure 8

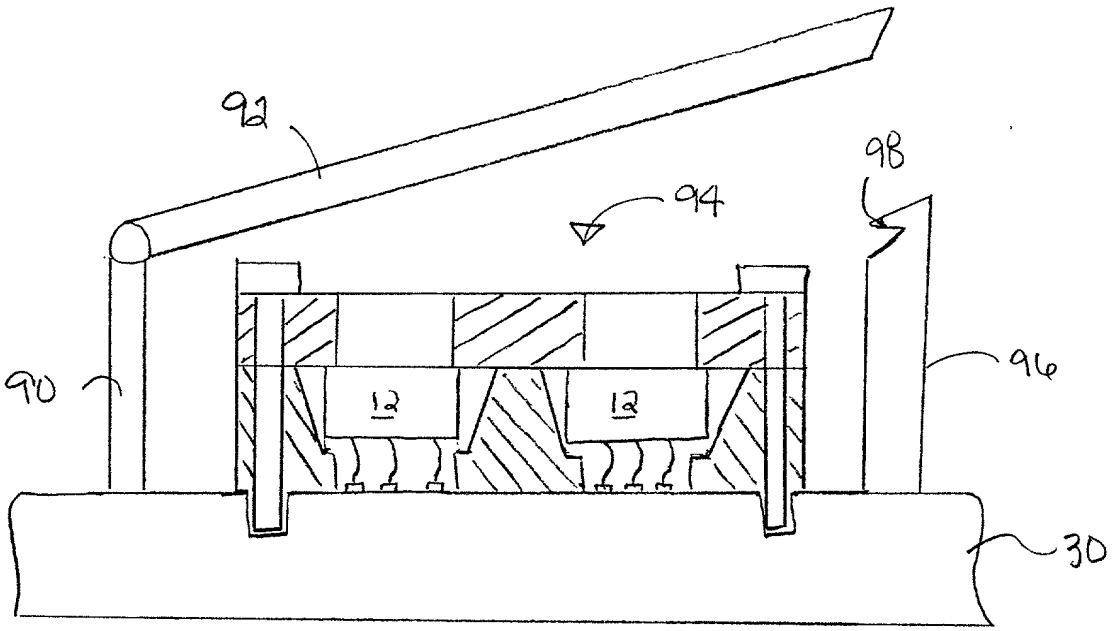


Figure 9A

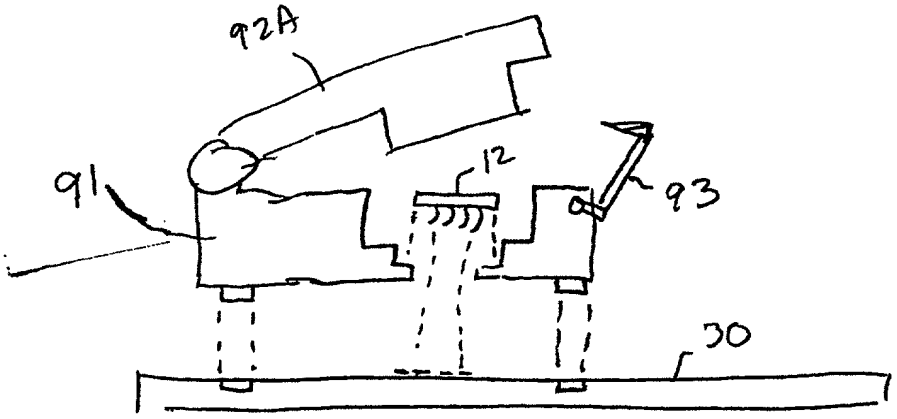
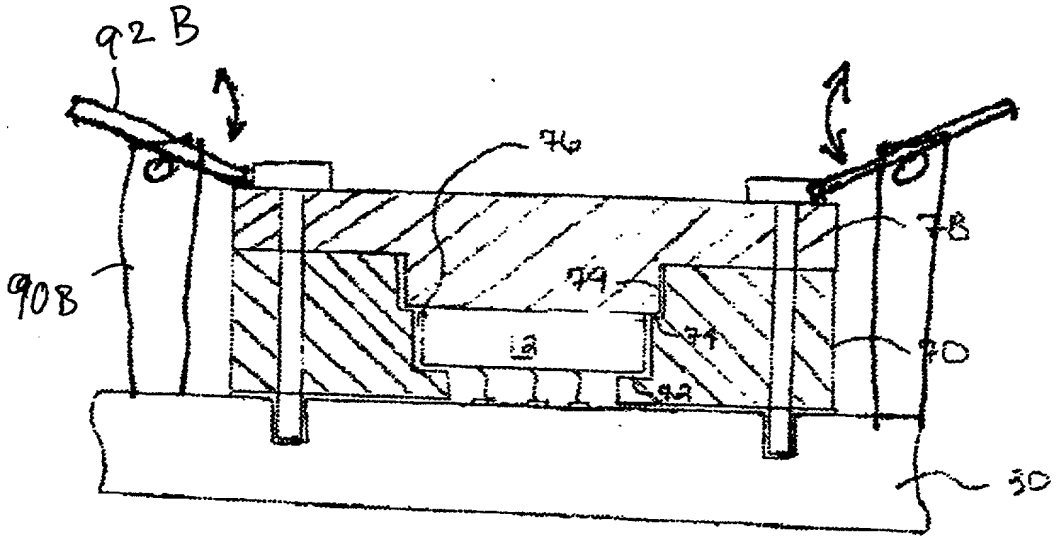
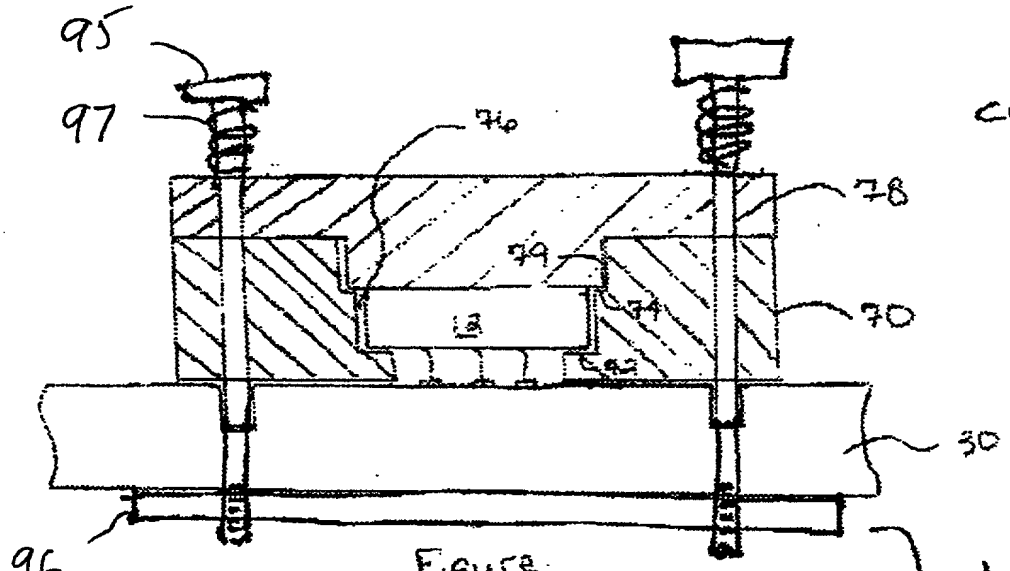


Figure 9B



Torsion Spring provides rotational force on lever arms

Figure 9C



compression springs

bolster plate

Figure 9D

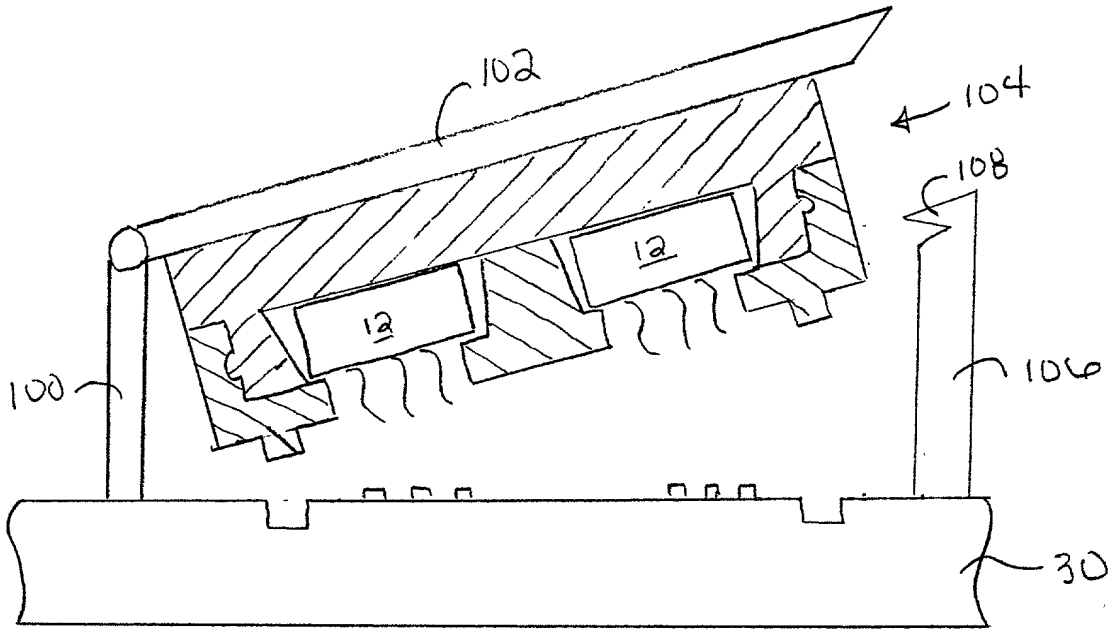


Figure 10

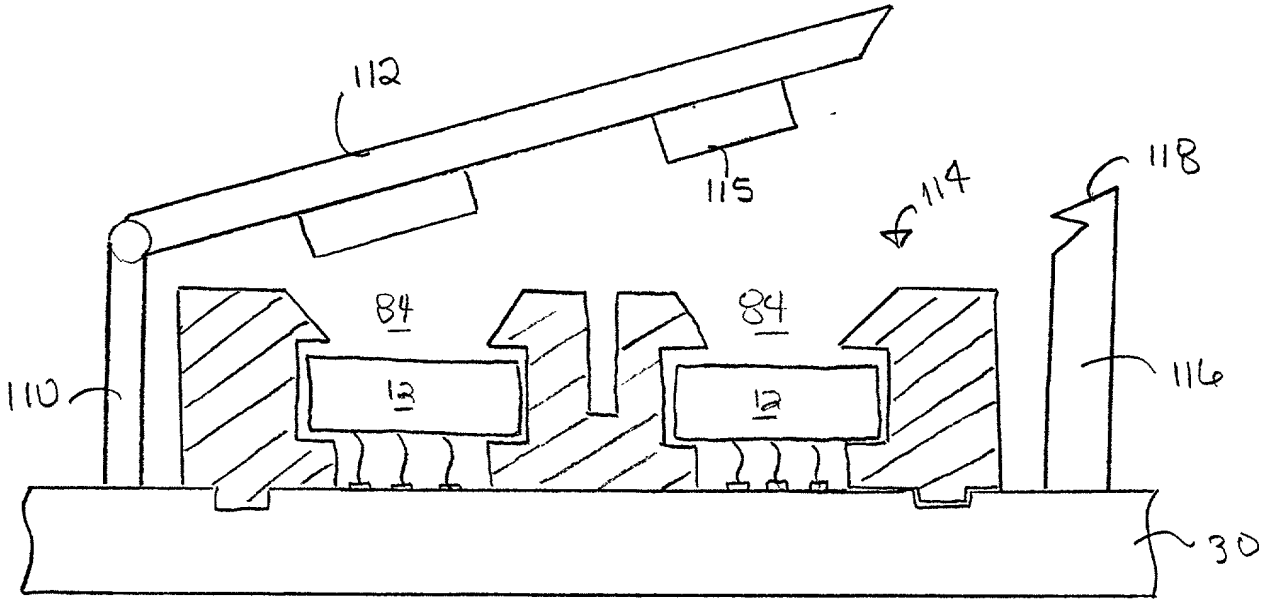


Figure 11

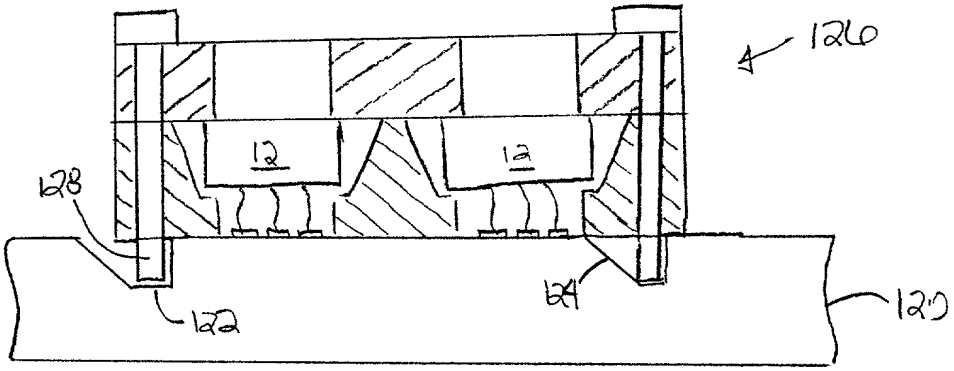


Figure 12A

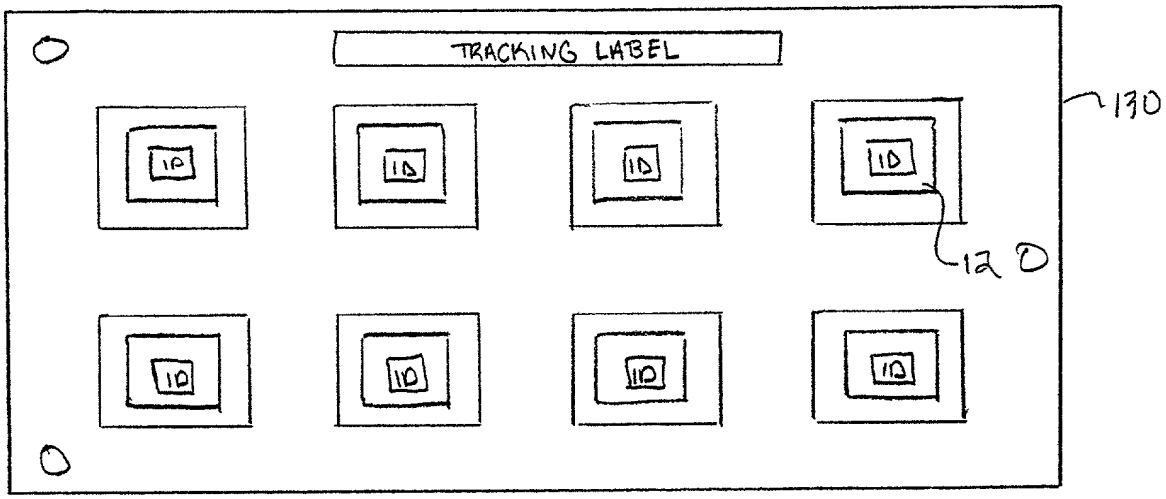


Figure 13A

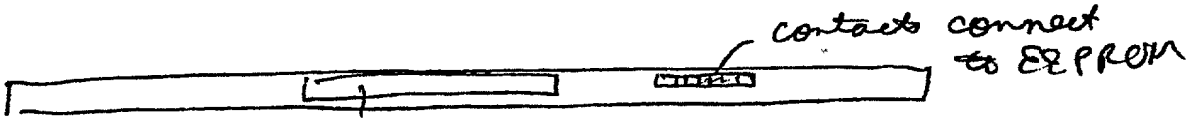


Fig. 13B

Figure 12B

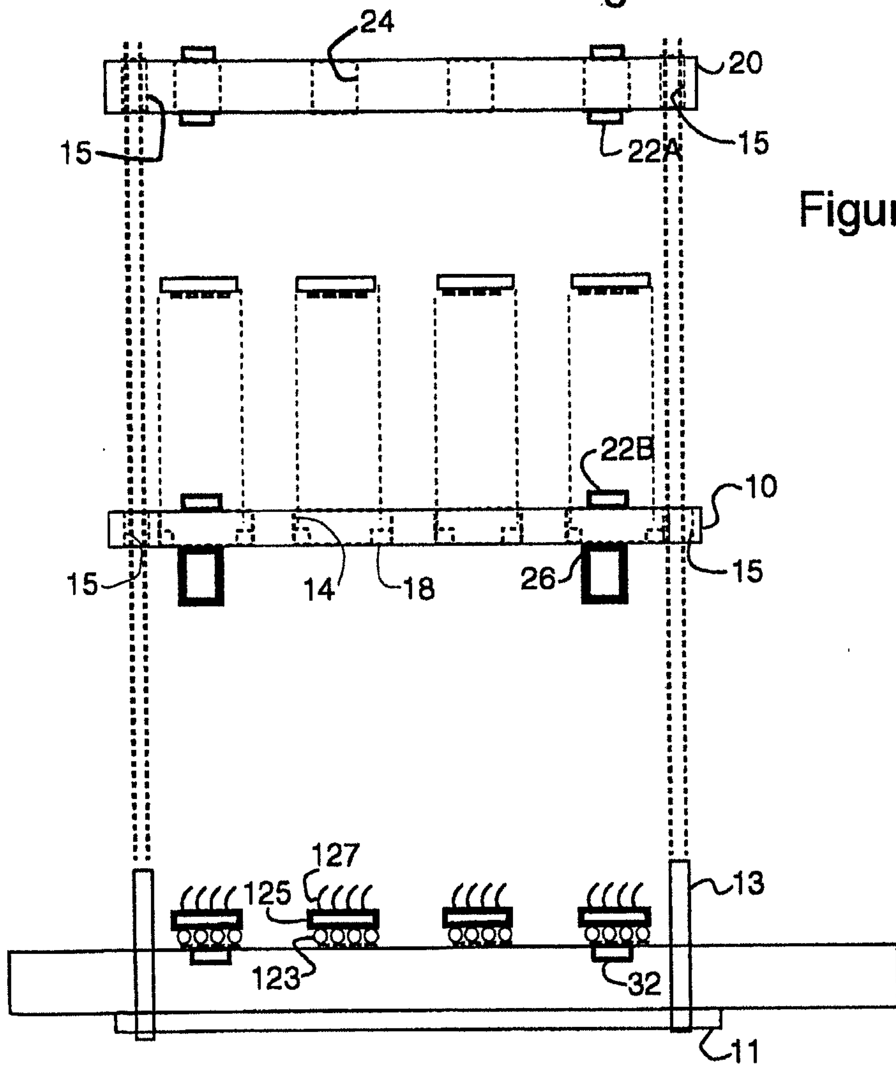


Figure 12C

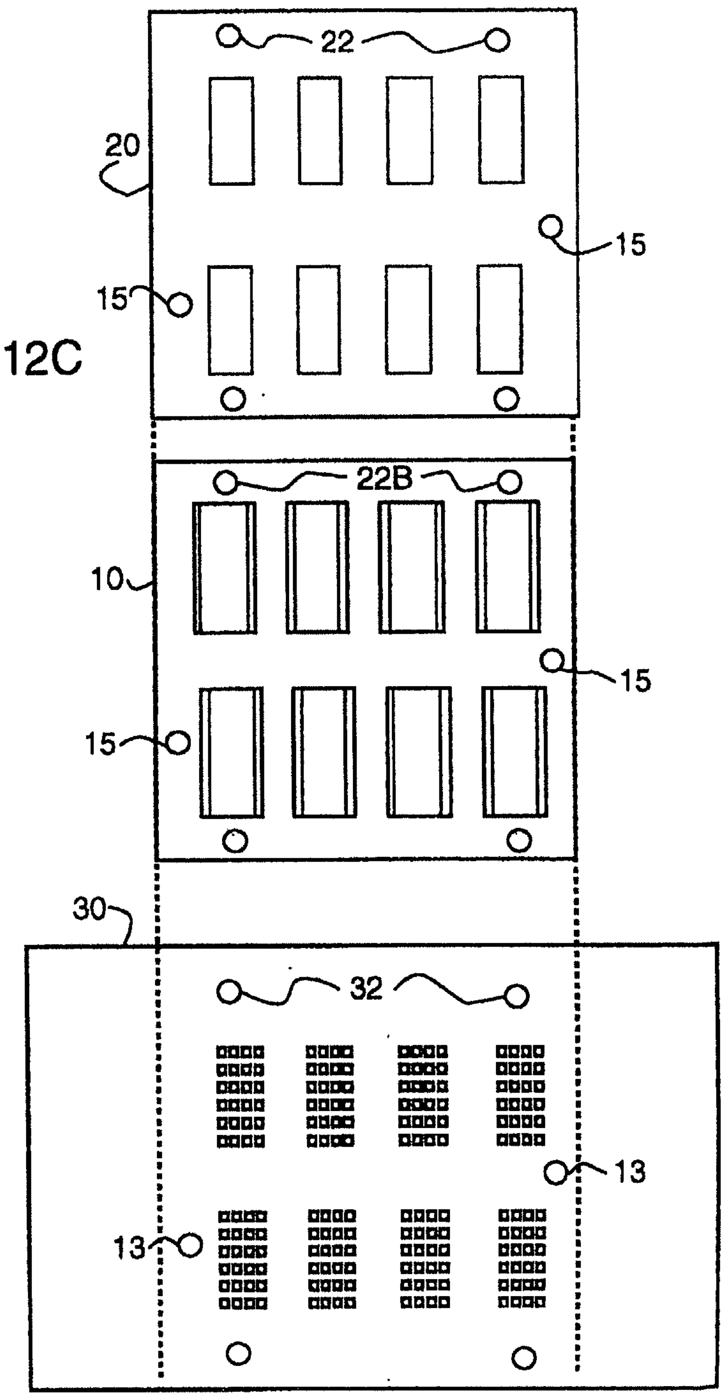
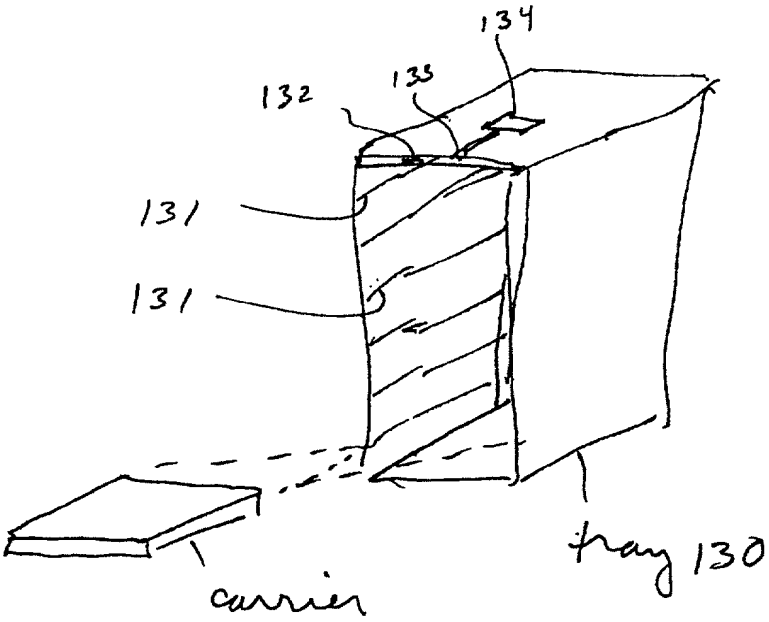


Figure 13C



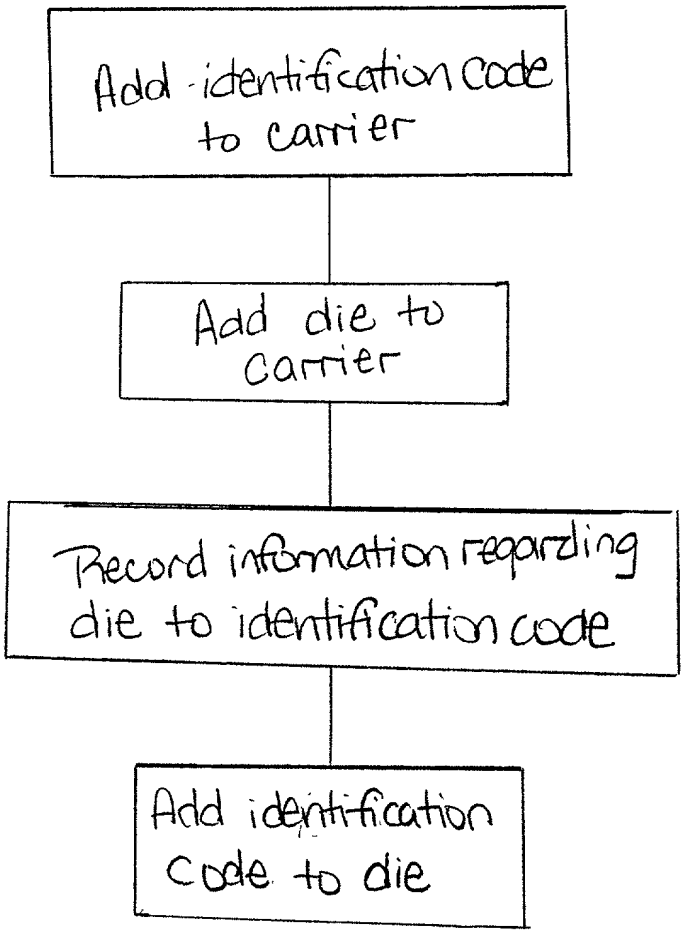

Add identification code to carrier
Add die to carrier
Record information regarding die to identification code
Add identification code to die

Figure 14

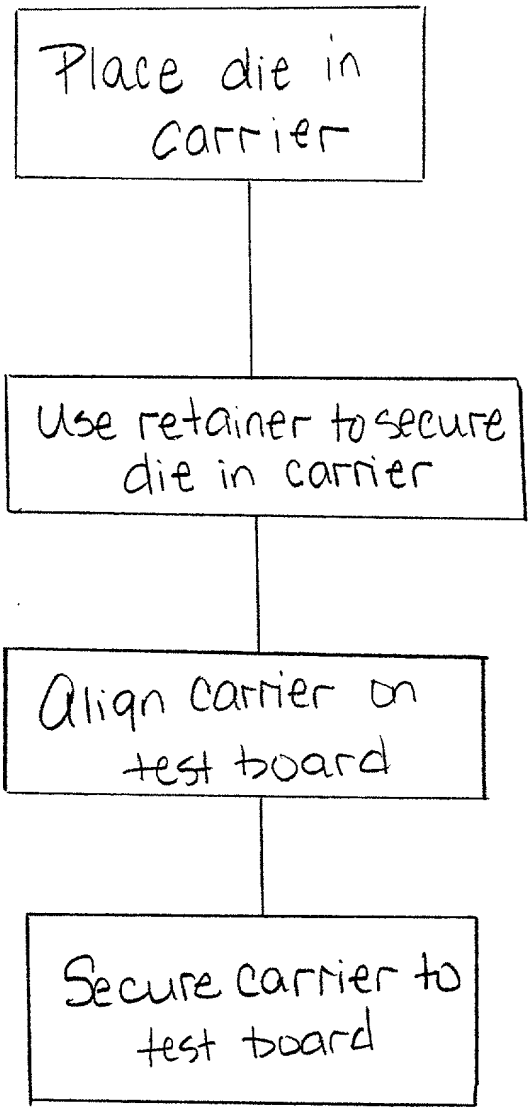

Place die in carrier
Use retainer to secure die in carrier
Align carrier on test board
Secure carrier to test board

Figure 15

Attorney's Docket No.: 03401.P090 PATENT

DECLARATION AND POWER OF ATTORNEY FOR PATENT APPLICATION
(CONTINUATION-IN-PART)

As a below named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated below, next to my name.

I believe I am the original, first, and sole inventor (if only one name is listed below) or an original, first, and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled

METHOD FOR PROCESSING AN INTEGRATED CIRCUIT

the specification of which

X is attached hereto.

_____ was filed on _____ as United States Application Number _____ or PCT International Application Number _____ and was amended on _____ (if applicable).

I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claims, as amended by any amendment referred to above.

I acknowledge the duty to disclose all information known to me to be material to patentability as defined in Title 37, Code of Federal Regulations, Section 1.56.

I hereby claim foreign priority benefits under Title 35, United States Code, Section 119(a)-(d), of any foreign application(s) for patent or inventor's certificate listed below and have also identified below any foreign application for patent or inventor's certificate having a filing date before that of the application on which priority is claimed:

Prior Foreign Application(s)			Priority Claimed	
(Number)	(Country)	(Day/Month/Year Filed)	Yes	No
(Number)	(Country)	(Day/Month/Year Filed)	Yes	No
(Number)	(Country)	(Day/Month/Year Filed)	Yes	No

I hereby claim the benefit under title 35, United States Code, Section 119(e) of any United States provisional application(s) listed below

(Application Number)	Filing Date
(Application Number)	Filing Date

I hereby claim the benefit under Title 35, United States Code, Section 120 of any United States application(s) listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by the first paragraph of Title 35, United States Code, Section 112, I acknowledge the duty to disclose all information known to me to be material to patentability as defined in Title 37, Code of Federal Regulations, Section 1.56 which became available between the filing date of the prior application and the national or PCT international filing date of this application:

09/205,502	**December 4, 1998**	**Pending**
(Application Number)	**Filing Date**	**(Status -- patented, pending, abandoned)**
(Application Number)	**Filing Date**	**(Status -- patented, pending, abandoned)**

I hereby appoint Farzad E. Amini, Reg. No. P42,261; Aloysius T. C. AuYeung, Reg. No. 35,432; Amy M. Armstrong, Reg. No. 42,265; William Thomas Babbitt, Reg. No. 39,591; Carol F. Barry, Reg. No. 41,600; Jordan Michael Becker, Reg. No. 39,602; Bradley J. Bereznak, Reg. No. 33,474; Michael A. Bernadicou, Reg. No. 35,934; Roger W. Blakely, Jr., Reg. No. 25,831; Gregory D. Caldwell, Reg. No. 39,926; Kent M. Chen, Reg. No. 39,630; Lawrence M. Cho, Reg. No. 39,942; Yong S. Choi, Reg. No. P43,324; Thomas M. Coester, Reg. No. 39,637; Roland B. Cortes, Reg. No. 39,152; Barbara Bokanov Courtney, Reg. No. 42,442; Michael Anthony DeSanctis, Reg. No. 39,957; Daniel M. De Vos, Reg. No. 37,813; Robert Andrew Diehl, Reg. No. 40,992; Tarek N. Fahmi, Reg. No. 41,402; James Y. Go, Reg. No. 40,621; Richard Leon Gregory, Jr., Reg. No. 42,607; Dinu Gruia, Reg. No. P42,996; David R. Halvorson, Reg. No. 33,395; Thomas A. Hassing, Reg. No. 36,159; Phuong-Quan Hoang, Reg. No. 41,839; Willmore F. Holbrow III, Reg. No. P41,845; George W Hoover II, Reg. No. 32,992; Eric S. Hyman, Reg. No. 30,139; Dag H. Johansen, Reg. No. 36,172; William W. Kidd, Reg. No. 31,772; Michael J. Mallie, Reg. No. 36,591; Andre L. Marais, under 37 C.F.R. § 10.9(b); Paul A. Mendonsa, Reg. No. 42,879; Darren J. Milliken, Reg. 42,004; Thinh V. Nguyen, Reg. No. 42,034; Kimberley G. Nobles, Reg. No. 38,255; Michael A. Proksch, Reg. No. 43,021; Babak Redjaian, Reg. No. 42,096; James H. Salter, Reg. No. 35,668; William W. Schaal, Reg. No. 39,018; James C. Scheller, Reg. No. 31,195; Anand Sethuraman, Reg. No. P43,351; Charles E. Shemwell, Reg. No. 40,171; Maria McCormack Sobrino, Reg. No. 31,639; Stanley W. Sokoloff, Reg. No. 25,128; Allan T. Sponseller, Reg. No. 38,318; Judith A. Szepesi, Reg. No. 39,393; Vincent P. Tassinari, Reg. No. 42,179; Edwin H. Taylor, Reg. No. 25,129; George G. C. Tseng, Reg. No. 41,355; Lester J. Vincent, Reg. No. 31,460; John Patrick Ward, Reg. No. 40,216; Stephen Warhola, Reg. No. 43,237; Charles T. J. Weigell, Reg. No. 43,398; Ben J. Yorks, Reg. No. 33,609; and Norman Zafman, Reg. No. 26,250; my attorneys, and James A. Henry, Reg. No. 41,064; Daniel E. Ovanezian, Reg. No. 41,236; Glenn E. Von Tersch, Reg. No. 41,364; and Chad R. Walsh, Reg. No. 43,235; my patent agents, of BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP, with offices located at 12400 Wilshire Boulevard, 7th Floor, Los Angeles, California 90025, telephone (310)

207-3800, and James R. Thein, Reg. No. 31,710, my patent attorney; with full power of substitution and revocation, to prosecute this application and to transact all business in the Patent and Trademark Office connected herewith.

Send correspondence to James C. Scheller, Jr., BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP, 12400 Wilshire Boulevard 7th Floor, Los Angeles, California 90025 and direct telephone calls to James C. Scheller, Jr., (408) 720-8598.
(Name of Attorney or Agent)

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

Full Name of Sole/First Inventor Douglas S. Ondricek

Inventor's Signature _____ Date _____

Residence Lafayette, California (City, State) Citizenship United States (Country)

Post Office Address 3359 Sweet Drive
Lafayette, CA 94549

Full Name of Second/Joint Inventor David V. Pedersen

Inventor's Signature _____ Date _____

Residence Scotts Valley, California (City, State) Citizenship United States (Country)

Post Office Address 6 Sterling Lane
Scotts Valley, CA 95066

Title 37, Code of Federal Regulations, Section 1.56
Duty to Disclose Information Material to Patentability

(a) A patent by its very nature is affected with a public interest. The public interest is best served, and the most effective patent examination occurs when, at the time an application is being examined, the Office is aware of and evaluates the teachings of all information material to patentability. Each individual associated with the filing and prosecution of a patent application has a duty of candor and good faith in dealing with the Office, which includes a duty to disclose to the Office all information known to that individual to be material to patentability as defined in this section. The duty to disclosure information exists with respect to each pending claim until the claim is cancelled or withdrawn from consideration, or the application becomes abandoned. Information material to the patentability of a claim that is cancelled or withdrawn from consideration need not be submitted if the information is not material to the patentability of any claim remaining under consideration in the application. There is no duty to submit information which is not material to the patentability of any existing claim. The duty to disclosure all information known to be material to patentability is deemed to be satisfied if all information known to be material to patentability of any claim issued in a patent was cited by the Office or submitted to the Office in the manner prescribed by §§1.97(b)-(d) and 1.98. However, no patent will be granted on an application in connection with which fraud on the Office was practiced or attempted or the duty of disclosure was violated through bad faith or intentional misconduct. The Office encourages applicants to carefully examine:

(1) Prior art cited in search reports of a foreign patent office in a counterpart application, and

(2) The closest information over which individuals associated with the filing or prosecution of a patent application believe any pending claim patentably defines, to make sure that any material information contained therein is disclosed to the Office.

(b) Under this section, information is material to patentability when it is not cumulative to information already of record or being made or record in the application, and

(1) It establishes, by itself or in combination with other information, a prima facie case of unpatentability of a claim; or

(2) It refutes, or is inconsistent with, a position the applicant takes in:

(i) Opposing an argument of unpatentability relied on by the Office, or

(ii) Asserting an argument of patentability.

A prima facie case of unpatentability is established when the information compels a conclusion that a claim is unpatentable under the preponderance of evidence, burden-of-proof standard, giving each term in the claim its broadest reasonable construction consistent with the specification, and before any consideration is given to evidence which may be submitted in an attempt to establish a contrary conclusion of patentability.

(c) Individuals associated with the filing or prosecution of a patent application within the meaning of this section are:

(1) Each inventor named in the application;

(2) Each attorney or agent who prepares or prosecutes the application; and

(3) Every other person who is substantively involved in the preparation or prosecution of the application and who is associated with the inventor, with the assignee or with anyone to whom there is an obligation to assign the application.

(d) Individuals other than the attorney, agent or inventor may comply with this section by disclosing information to the attorney, agent, or inventor.